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Three-Transistor Antifuse OTP Memory: Design, Simulation and Behavioral Verification

Jyoti Thakur, Bhavesh Soni

Abstract: ***This paper presents the plan for modelling and behavioural verification of a three-transistor antifuse-based One-Time Programmable (OTP) memory cell. This was execute using Verilog HDL and simulated within the Xilinx ISE 14.7 environment. This is a combination of an NMOS antifuse, a high-voltage blocking transistor, and an access transistor, which together enable permanent data storage through gate-oxide breakdown. A behavioural Verilog model is generated during the programming stage to change the antifuse resistance permanently. Its functionality was proved using ISim simulations. The simulations demonstrate reliable one-time programmability, stable data retention, or clear differentiation between programmed and unprogrammed states. Programming is achieved by activating the prog_en and vg_bt signals to lock the otp_bit node, followed by consistent read operations using the word line (wl) and bit line (bl). This memory cell is well-suited for System-on-Chip (SoC) integration, particularly for applications requiring secure cryptographic keys, unique device identifiers, calibration parameters, and configuration storage. The use of standard Verilog promotes rapid FPGA prototyping and seamless system deployment.***

Keywords: ***3T OTP Memory Cell, Antifuse-Based Memory, Verilog HDL Modelling, Gate Oxide Breakdown, Non-Volatile Storage, Xilinx ISE Simulation, One-Time Programmable, High-Voltage Blocking Transistor, Read Disturb Mitigation, SoC Integration.***

Nomenclature:
OTP: One-Time Programmable
NVM: Non-Volatile Memory
IoT: Internet of Things
SoC: System-On-Chip
PUF: Physically Unclonable Functions
DUT: Device Under Test
BL: Bit Line

I. INTRODUCTION

One-Time Programmable (OTP) memory is an important component in modern VLSI systems for secure and permanent data storage. In contrast to reprogrammable memories such as EEPROM, Flash OTP helps protect data against tampering. This makes it suitable for storing encryption keys, authentication codes, calibration data, and firmware in power ICs.

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LCD drivers and image sensors. Due to its non-volatile nature, data in OTP memory remains even when power is off, which is crucial for security-related applications. Today, ICs utilise various memory types to meet stringent requirements for power, size, and security in mobile processors and IoT devices. OTP memory is helpful for its permanence, reliability and compatibility with CMOS technology. Among the different types of OTP antifuse designs, those are preferred over traditional fuses because they require smaller cells, consume less power, and offer easier integration into the manufacturing process. Antifuse cells function by establishing a permanent low-resistance path through controlled gate-oxide breakdown, which results in resistances detectable by standard sensing circuits.

The 3T cell design, which combines an NMOS antifuse, a high-voltage blocker, and an access transistor, enhances reliability by shielding the read path from programming stress. Although using very thin oxides (less than 40 Å) can lead to variable resistances and yield issues. The blocker helps ensure that.

Only the selected cells experience stress. Verilog HDL facilitates verification in digital design processes. Xilinx ISE 14.7 can be used for simulation and FPGA prototyping of OTP cells without requiring access to a fabrication facility [1].

II. LITERATURE REVIEW AND BACKGROUND

A. Memory Fundamentals

Memory plays is the electronic space where information is stored. Often referred to as the heart of a system, memory can store information temporarily or permanently, depending on its type. In embedded systems and other electronic devices, memory allows the tracking and storage of programs and the management of current tasks.

The functions of memory are diverse: To store data that is to be processed by the CPU. Basic functions include encoding, storing and retrieving information. It helps with planning, comprehension, and reasoning.

i. *Types of Memory*

Memory can be divided into volatile and non-volatile based on data retention after power loss. This is important for designers when choosing memory for specific applications. Volatile Memory requires continuous power to retain stored information, making it suitable for temporary data used during active processes.

ii. *The Main Types Include*

- SRAM (Static RAM): Type of semiconductor memory that uses flip-flop (bistable) to store each bit
- DRAM (Dynamic RAM): Random-access semiconductor memory that stores

each bit of data in a separate tiny capacitor within an IC.

Non-Volatile Memory retains data even when power is off, making it important for storing boot instructions and long-term information.

- ROM (Read-Only Memory): Temporary memory that holds information while powered on.
- PROM (Programmable ROM): Permanent memory that holds data even when powered off.
- OTP (One-Time Programmable) Memory: A type of memory that can be programmed using a suitable programming device. Once programmed, it cannot be removed.

iii. Importance of Non-Volatile Memory

Non-volatile memory (NVM) refers to a type of computer storage that retains data. Unlike volatile memory, NVM stores important data such as system configurations, calibration settings, and event logs during power interruptions [4]. This function plays an important role in devices such as industrial controllers and smart meters, where maintaining operational data and historical records for extended periods is required. NVM is responsible for storing boot code and firmware, which help devices start immediately after power is applied. Memory technologies have evolved from inflexible mask ROM to more adaptable options, such as Flash and One-Time Programmable (OTP) memory, which enable updates to accommodate field changes. However, corruption in NVM can lead to significant issues, including complete system failure. For security reasons, NVM securely stores encryption keys, device identifiers, and digital certificates through tamper-resistant one-time programming. This capability is critical for secure boot processes, device authentication in the Internet of Things (IoT), cryptographic operations in mobile devices and payment systems [5]. NVM can also reduce the need for backup batteries, resulting in more compact and cost-effective designs, particularly in high-volume IoT and consumer products. OTP memory is especially well-suited to harsh environments, such as extreme temperatures, offering long-term data retention through irreversible structural changes. This makes it a dependable option for automotive, industrial, and aerospace applications. NVM features zero standby power consumption and minimal current draw during read operations, making it suitable for battery-operated IoT sensors and wearable devices. Its programmability allows late-stage modifications across multiple hardware variants, accelerating product development compared to traditional mask ROM. These features position OTP memory as a strong option for permanent, secure data storage in modern connected systems that utilise advanced CMOS technologies.

B. OTP Memory Fundamentals

One-Time Programmable (OTP) memory may be a non-volatile memory type that permits information to be written once, after fabrication. Once modified, information is locked in and put through a physical alteration within the memory cell, making it permanent and unalterable. Unlike EEPROM or Streak, which support numerous program and erase cycles, OTP memory retains data for 10 to 20 years or more, making it ideal for storing encryption keys, verification codes, calibration values, configuration information, secure firmware, and device IDs.

Key points of interest of OTP memory include its resistance to alteration, its capacity to hold information without control, its clear integration into standard CMOS forms, its compact cell structures for high-density and high endurance without the need for information revival, and its quick read/write speeds for arrangement tasks and cost-effectiveness.

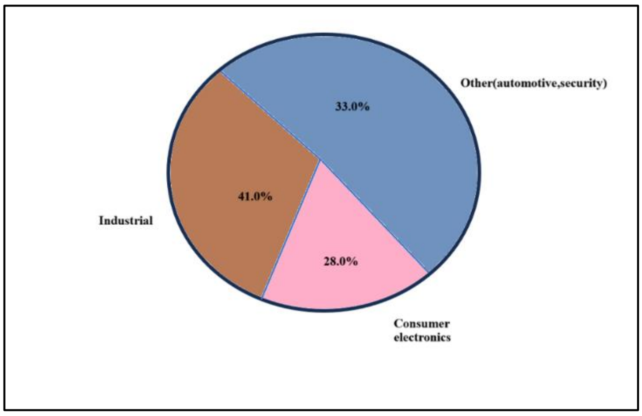
i. OTP Memory Type :

eFuse-based technology is a type of OTP memory. It uses small bits and fuses that change permanently when programmed. A specific voltage is used to blow the fuse.

An antifuse OTP creates conductive paths when programmed. A higher-voltage connection permanently connects the circuit.

Erase and Antifuse are the two techniques used in OTP memory. Here is how they compare;

An E fuse uses high current to break a connection (link), making it well-suited for manufacturing adjustments. An antifuse creates a connection (link), which makes it ideal for irreversible tasks.



[Fig.1: Illustrates the Market Trajectory of One-Time Programmable (OTP) Memory]

C. Antifuse Technology

i. Operating Principle

Antifuse memory innovation employs the electrical breakdown of thin oxide layers in standard CMOS devices. At first, the antifuse acts as an awfully high-resistance gadget (over 1 GΩ). When operated at a high voltage, it permanently switches to a low-resistance state in the kilo-ohm range—the opposite of a combination, which becomes an open circuit when triggered[6].

An ordinary antifuse cell is shaped like a MOS transistor, with the source, drain, and body tied together. In contrast, the entryway oxide (around 15–50 Å thick) serves as the dielectric isolating the door from the common hub. For example, a 0.18 µm handle might utilise a 38 Å oxide that protects under ordinary conditions but breaks down at voltages around 5–6 V.

Applying this programming voltage produces a strong electric field within the oxide, which affects ionisation and the formation of conductive fibres through the oxide layer. This preparation physically transforms the separators into an unchanging conductor. The cell with intaglio oxide is examined as a rationale '0', whereas the modified, shortened cell is identified as a rationale '1'. This strategy leverages the existing CMOS entryway structure, resulting in compact, robust, and cost-effective OTP memory for an implantable framework setup.

ii. Breakdown Mechanism

The performance of antifuse OTP memory depends on achieving complete oxide breakdown. As the electric field increases, electrons can tunnel through the oxide (Fowler-Nordheim tunnelling). At higher fields, ionisation creates additional carriers and neighbourhood charge traps, thereby accelerating the breakdown process. Two breakdown modes result: delicate and difficult.

A delicate breakdown causes partial conduction and unstable resistance, leading to unreliable readings and potential information errors. Hence, the OTP antifuse plan guarantees that the conditions continuously lead to a difficult breakdown. In a difficult breakdown, a steady, unchanging conductive fibre shapes, providing the cell with a steady, low resistance that guarantees reliable detection and long-term maintenance.

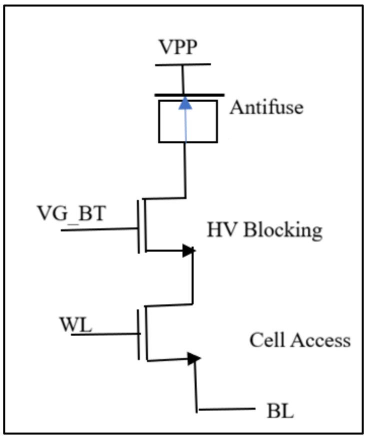
iii. Programming and Reading

Programming the antifuse requires carefully controlled high voltage to focus on cells, as it were. Chosen cells have their word line empowered, the bit line grounded, and a blocking transistor sets the correct voltage drop. The programming voltage (VPP) is ramped up to the cell's breakdown voltage, causing the fibre to form. Brief beats and current limits help prevent overheating. Once modified, the cell remains within the low-resistance (rationale '1') state; unprogrammed cells stay unaffected.

Perusing is performed at normal supply voltages, much lower than those used for programming, ensuring the cell's state isn't disturbed. During readout, the selected word line is driven, and the bit lines are precharged. Modified cells permit current to flow, releasing the bit line and lowering its voltage, which is interpreted as a logic '1'. Unprogrammed cells with oxide generate current and maintain high voltage. The significant resistance difference ensures reliable data, covering variations in process voltage and temperature, typically using simple sensing circuitry.

III. THREE-TRANSISTOR ANTIFUSE OTP CELL ARCHITECTURE

A. Cell Components and Structure



[Fig.2: 3T OTP Cell]

The 3-transistor antifuse OTP memory cell consists of a thin-oxide NMOS antifuse, a high-voltage blocking transistor, and an access transistor. This configuration enables definitive programming, consistent readout, and efficient use of chip area [2]. The antifuse is a thin-oxide NMOS device with its source, drain, and body connected to form a two-terminal structure. The gate of this transistor receives a programming voltage (VPP), while the common node is connected to a blocking transistor. In its unprogrammed state, the oxide acts as an insulator with high resistance, which stops current flow. When a programming voltage is applied, this causes a physical breakdown of the oxide, establishing a permanent, low-resistance path. A thick-oxide blocking transistor is positioned between the antifuse and the access transistor. During programming, the gate is set to an intermediate voltage, allowing safe current flow and reducing excess voltage so that the high programming voltage can reach the antifuse without damaging other circuit components. The access transistor, controlled by the word line, connects the cell's internal node to the bit line during programming and reading. When activated, it connects the cell to the bit line; when not selected, it isolates the cell from the column circuitry. Its size is minimised to decrease capacitance while still providing sufficient current for reliable reading. This cell design supports dense memory arrays, protects unselected cells from unintended programming, and is compatible with standard CMOS manufacturing processes.

B. Operation Modes

The 3T antifuse OTP cell is used in two fundamental modes, each with specific voltage conditions to ensure proper operation and data integrity [3].

i. Programming Mode:

To program a chosen cell, the word line is asserted, the bit line is held at ground, the gate of the blocking transistor is set to a half-level, and a high voltage is connected to the antifuse input. This causes the oxide to break down, forming a conductive path and, over time, lowering the cell's resistance. As it were, the focused-on cell is modified, while dormant word lines or confined bit lines ensure that unselected cells remain unselected.

ii. Reading Mode:

When perusing, the programming voltage is set to typical supply levels, and the blocking transistor is fully on. The word line is raised to be put through the cell to the bit line, which has been precharged tall. In case the cell is modified, current streams and discharges the bit line (rationale '1'); on the off chance that it is unprogrammed, current spillover is irrelevant, and the bit line remains high (rationale '0'). Non-selected cells remain cut off from the operation under review.

iii. Programming Process:

Programming is carefully overseen through push and column choice. The chosen row's word line is raised, turning on the transistors and interfacing each cell to its bit line. As it were, the target column's bit line is grounded, keeping current to the aiming cell. The blocking transistor's door is set to a middle position, constraining current and ensuring that the voltage at the inner hub doesn't exceed the gate-to-transistor breakdown rating. The programming voltage increases on the antifuse door, causing oxide breakdown and fibre alignment. As resistance drops, the current self-limits. Once the method completes, all voltages are reset, and the cell is forever modified.

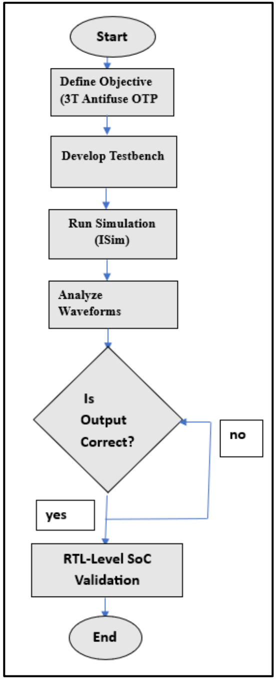
iv. Read Process:

Perusing employment at only low voltages to avoid any unsettling influence on cell information. All bit lines are precharged tall. The chosen row's word line is actuated, interfacing the cells to their bit lines, while the blocking transistors are fully on. Modified cells permit current to stream, rapidly releasing the bit line (rationale '1'), whereas unprogrammed cells scarcely spill, keeping the bit line tall (rationale '0'). The wide contrast in resistance between these states guarantees dependable discovery, indeed across variations in manufacturing or natural conditions. After the analysis is completed, word lines fall, and bit lines are precharged again, with the entire cycle taking a few hundred nanoseconds.

IV. METHODOLOGY

A. Design Overview

This project demonstrates a 3T antifuse OTP cell using behavioural modelling in Verilog HDL, with simulations executed in Xilinx ISE 14.7. The workflow constructs a digital model that represents single-use programming, non-volatile data retention, and read operations, simplifying the underlying physical mechanisms for RTL-level design. The step includes creating a Verilog module, setting up a testbench, running simulations with ISim and analysing waveforms to ensure correct operation. The focus is on ensuring that the cell undergoes a permanent state change after programming and that a clear distinction exists between programmed and unprogrammed states during readout. This approach enables early verification in system-on-chip (SoC) projects without requiring detailed device or analogue simulations [7].



[Fig.3: Flow]

B. Three-Transistor Antifuse OTP Cell Design in Verilog

The 3T antifuse OTP cell is depicted in Verilog using behavioural modelling, translating the physical programming process straightforwardly and clearly into digital state transitions. This approach models antifuse blocking and access circuitry with logic that reflects cell one-time programmability and permanent data retention.

Module interfaces include a programming enable input (prog_en), a control for the blocking transistor (vg_bt), a word line input (wl) for the access transistor, and a bidirectional bit line (bl) capable of tri-state operation. For the programming model, an internal otp_bit register is initialised to '0' to indicate an unprogrammed state. When both prog_en and vg_bt are active on a positive clock edge, the otp_bit is set to '1' and remains latched, reflecting the irreversible change in an actual antifuse cell. This edge-triggered mechanism prevents unintended state changes.

For reading, when WL is high, the model drives the bit line with the value of otp_bit; when WL is low, the bit line is in high impedance, enabling multiple cells to share the same line in a memory array. This read logic is combinational and asynchronous in line with standard OTP access methods. The RTL model indicates the construction of a single cell, the 3T cell.

C. Testbench Design in Verilog

The testbench rigorously verifies the 3T antifuse OTP cell across all operational modes using Verilog test stimuli and ISim simulation waveforms.

Setup: The testbench defines all cell inputs and outputs. Creates an instance of the device under test (DUT)and sequences test events in an initial block with suitable delay intervals for signal stabilization. The bit line (bl) is continuously monitored, and the testbench records the pass/fail status for each check.

i. Test Steps:

- Initial Read: The word line is set high, and the bit line should read '0', confirming the cell's default unprogrammed state.
- Programming: prog_en and vg_bt are pulsed while the word line stays low, which causes the internal otp_bit to change to '1' to simulate programming.
- Post-Programming Read: With the word line high again, the bit line outputs '1', verifying that the programmed state is retained.
- Reprogram Attempt: A second pulse on prog_en and vg_bt does not change the state, demonstrating the one-time programmable characteristic.
- Repeated Reads: Multiple activations of the word line consistently yield bl = '1', indicating stable retention and repeatable readout.

Display statements flag each step, while waveform analysis confirms proper timing, permanent state changes, and immunity to disturbances. Waveform configurations are archived for future reference, and images are exported for documentation. These results confirm the cell's single-programming capability for long-term data retention and dependable reading.

D. Xilinx ISE Simulation Setup

3T antifuse OTP cell was implemented and authenticated using Xinix ISE

14.7.Employing Verilog HDL and the Isim simulator. The RTL level confirmed accurate single-use programming, data retention, consistent read performance, and integration into a larger SOC project.

The Verilog module for the cell and testbench are designed to enable behavioural simulation, which allows rapid execution and simple waveform inspection without the requirement for extensive gate-level or physical layout modelling. The internal otp_bit register of the cell indicated the permanent state-change result of programming, simplifying the breakdown mechanism into a digital model.

Simulations with Isim were executed using a 1ns/100ps timescale and lasted for several hundred nanoseconds, including initialisation, programming, reading, and reprogramming attempts. Given that the design is asynchronous. A clock was not required instead the testbench utilized explicit resets to establish a known starting state.

In the ISE Project Navigator progression, included creating a new project, adding Verilog source files, performing syntax checks through synthesis, and selecting "Simulate Behavioural Model." Console output displayed testbench messages and waveforms for prog_en, vg_bt, wl, bl, and otp_bit were automatically generated for analysis. No timing constraints were necessary for this level of functional checking.

E. Main Finding from the Waveforms:

- i. *Initial Read:* The bit line was '0', indicating the cell was unprogrammed.
- ii. Programming *Pulse*: With prog_en and vg_bt both high, otp_bit changed from '0' to '1'.
- iii. Post-*program Read:* The bit line (bl) output '1 specifies that the programmed state was retained.
- iv. *Reprogram Attempt:* No change in otp_bit, confirming that the cell cannot be reprogrammed.
- v. *Multiple Reads:* The bit line remained at '1', demonstrating stable retention and consistent readout.

V. RESULTS AND DISCUSSION

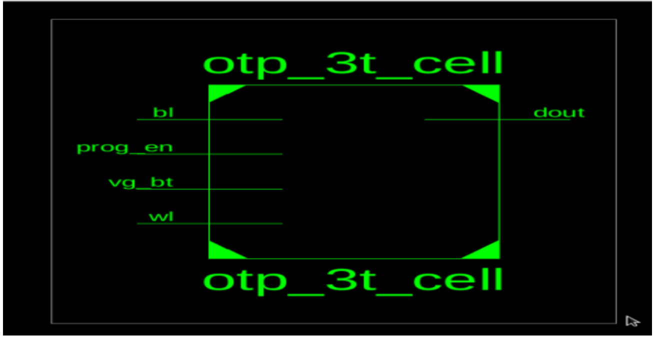
Behavioural reenactment with Xilinx ISim confirmed the proper operation of the 3T antifuse OTP cell. The results demonstrated the expected default state, successful one-time programming, reliable data retention, accurate readout, and resistance to reconstruction. Waveform analysis over a 150 ns interval validated each mode of operation with precise timing.

At the start of the recreation (t=0), all signals were set to moo (prog_en=0, vg_bt=0, wl=0), and otp_bit was initialized to 0, indicating the unprogrammed, high-resistance state. At t=10ns, the initial signal (wl tall) yielded dout=0, confirming the standard state without any disturbances. Programming took place between t=20-30ns with changes to prog_en and vg_bt (wl moo), resulting in otp_bit changing to 1 and remaining locked, indicating a permanent state transition.

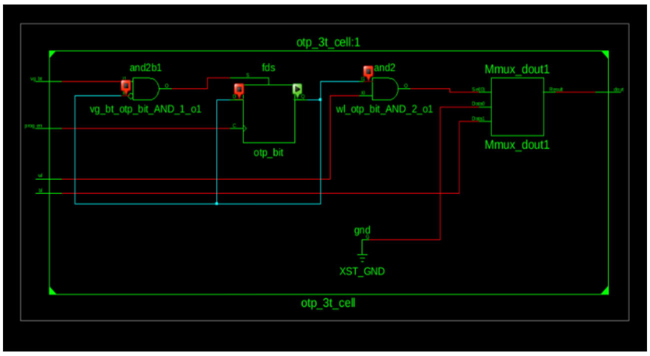
A subsequent read at t=40ns (with a write latency of tall) resulted in dout=1, confirming a distinct difference between states and reliable, non-destructive detection. An attempt to reconstruct at t=60-70ns left otp_bit unchanged at 1; a read at t=80ns again confirmed dout=1. Additional read cycles (t=80-120ns, five 5ns write pulses) consistently showed dout=1 without any glitches or data loss, demonstrating reliable read persistence.

This comes about: the cell peruses as if unprogrammed; a dual-signal program sets it to 1 for all time; perusing does not exacerbate the state; and reconstructing is outlandish. This RTL show is confirmed for use in SoC plans with array-level integration.

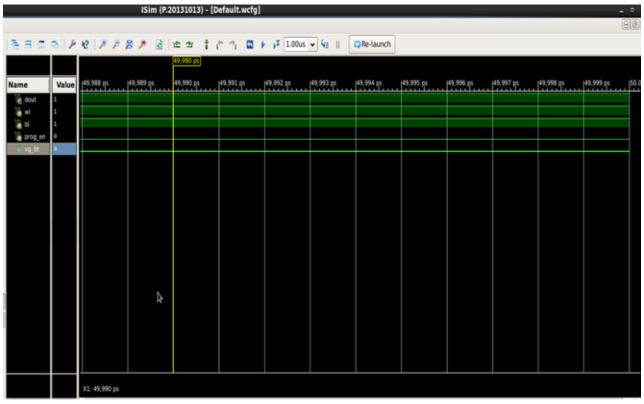
The recreation waveforms clearly outline all the specified highlights: an introductory unprogrammed state of zero, fruitful programming to one, non-volatile maintenance after programming, failure to reconstruct, and steady, repeatable perused execution.



[Fig.4: Xilinx ISE Design Summary]



[Fig.5: Xilinx ISE Project Navigator - RTL View]



Name	Value
dout	1
wl	1
bl	1
prog_en	0
vg_bt	0

[Fig.6: Simulation Waveform Results]

VI. CONCLUSION

The Verilog-based plan for the 3T antifuse OTP cell was thoroughly tested in ISim and demonstrated irreversible programming from 0 to 1, long-term maintenance, dependable operation, and total resistance to reconstruction. Introductory peruses affirmed the cell's rationale state when unprogrammed, whereas post-programming peruses reliably occur in a steady rationale 1 with a clear partition between states.

Endeavours to reconstruct the cell had no effect, affirming the one-time programmable nature vital for secure capacity. Different studies of cycles showed that the cell might be reached more than once without corruption or information loss. The behavioural modelling approach effectively captured the physical behaviour, enabling rapid and viable RTL-level verification.

With this confirmed show, early integration into system-on-chip (SoC) ventures is bolstered for secure applications such as encryption key storage, device identification, and calibration — all within standard computerised design flows and without the need for analogue re-enactment instruments. This facility presently permits subsequent expansion into memory assemblies and the incorporation of supplementary logic.

VII. FUTURE WORK

With the 3T antifuse OTP cell shown approved, the next step is to scale to array-level memory by instantiating cell lattices in Verilog. This will include push and column decoders, multiplexers, and nonconcurrent address-to-data transformation circuits to enable larger memory modules ranging from kilobits to megabits. Coordination, strong sense intensifiers for dependable current detecting, and full control and I/O circuitry will permit comprehensive framework testing. FPGA emulation, especially on Xilinx platforms, will be used to compare the recreated results with actual equipment execution.

Encouraging refinement of the show, utilising techniques arising from Zest recreations and silicon estimations, will enable adjustment for both advanced FinFET and established CMOS forms. Custom physical format, counting plan, run-the-show checks, layout-versus-schematic confirmation, and parasitic extraction will guarantee that the memory macros are prepared for SoC integration. Unwavering quality will be assessed through corner investigations of temperature, supply voltage, and prepared varieties.

Future endeavours will also investigate elective memory designs, such as one- and two-transistor antifuse plans, as well as hybrid approaches that combine OTP and multi-time programmability using parallel antifuses or Streak technology. Upgraded security features—such as alter discovery, physically unclonable functions (PUF), and anti-reverse engineering measures—will be focused on for automotive, mechanical, and military use. In addition to reenactment, formal confirmation strategies will be integrated to meet the safety-critical application requirements.

DECLARATION STATEMENT

As the article's author, I must verify the accuracy of the following information after aggregating input from all authors.

- **Conflicts of Interest/ Competing Interests:** Based on my understanding, this article has no conflicts of interest.
- **Funding Support:** This article has not been funded by any organizations or agencies. This independence ensures that the research is conducted with objectivity and without any external influence.
- **Ethical Approval and Consent to Participate:** The content of this article does not necessitate ethical approval or consent to participate with supporting documentation.
- **Data Access Statement and Material Availability:** The adequate resources of this article are publicly accessible.
- **Author's Contributions:** The authorship of this article is contributed equally to all participating individuals.

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Prof. Bhavesh Soni serves as an Assistant Professor in the Department of Electronics and Communication Engineering at the U. V. Patel College of Engineering, Ganpat University, Gujarat, India. He holds a Master of Engineering (M.E.) in VLSI System Design, specialising in high-performance digital architectures. With over a decade of experience in academia, his primary research focus includes Low-Power VLSI Design, System-on-Chip (SoC) implementation, and advanced Embedded Systems. Prof. Soni has a significant research portfolio, having authored several papers in reputable international journals and conferences on topics ranging from power-aware verification methodologies to digital circuit optimisation. He is actively involved in mentoring postgraduate research scholars and contributes to the academic community through his expertise in industry-standard EDA tools and modern hardware description languages. His work bridges the gap between theoretical circuit design and practical, energy-efficient VLSI solutions.
