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Review of 6T SRAM for Embedded Memory Applications

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Abstract*: Due to the substantial impact embedded Static Random Access Memory (SRAM)s have on the overall system and their relatively limited design, it is essential to manage embedded SRAM trade-offs strategically. SRAMs have power, performance and density trade-offs in general. In all applications, all three dimensions are necessary to some extent; accordingly, embedded SRAM design must incorporate the most crucial system-specific requirements when developing embedded SRAM. This paper discusses many SRAM factors, including Static Noise Margin (SNM), Read Access Time (RAT), Write Access Time (WAT), Read Stability and Write Ability, Power, Data Retention Voltage (DRV), and Process Control. All these factors are crucial when designing SRAM for embedded memory applications. There has also been a discussion of the parameter comparisons and the literature review of the current papers.

Keywords: Area, Memory Application, Latency, Power, SNM, SRAM

I. INTRODUCTION

Memory functions similarly to the human brain. It keeps track of different kinds of information and data. The area in a computer where data and the instructions for processing them are stored is called the memory. Memory technologies have increased over the past three decades. There are currently two broad categories of memory technologies: volatile and non-volatile. Non-volatile memory keeps data even after turning off the device, while volatile memory does not. Currently, the three dominant storage technologies in the industry are SRAM, DRAM, and NAND flash. There are three possible modes for a SRAM cell: Rest while the circuit is not in use, reading when data is requested, and writing when it is necessary to update the content. Read-stability and write-ability should be present in the SRAM when used in read mode and write mode, respectively. Many microelectronic applications rely on SRAMs, from consumer wireless devices to server CPUs and multimedia systems, to System on Chip (SoC). Increasing performance and throughput requires additional on-chip memory in today's processors and SoCs. As memory size grows, the required level of reliability becomes harder to meet. It is the first challenge for advanced technology nodes' SRAMs.

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With upgraded CMOS technology nodes, the static and dynamic power consumption increases. SRAMs in advanced technology nodes face a second hurdle as a result. Low-voltage SRAM has a higher risk of bit-cell failure due to process variations. The most susceptible circuit to process changes is static random-access memory because it uses rigid design criteria to achieve the highest possible integration density. For SRAM to be stable, SNM plays crucial role. SRAM cell's SNM represents its ability to hold data against noise. An SRAM's static noise margin is a minimum voltage shown on its storing nodes required to flip a cell's state. [26]

II. PARAMETER OF SRAM

1. Static Noise Margin (SNM):

Designing SRAM cells requires consideration of two factors: their dimensions and sturdiness. The cell area accounts for roughly two-thirds of the entire chip area. At low supply voltages, full-CMOS cells have significantly higher SNM values than R-load cells. Comparing standard R-load cells to full-CMOS cells may reveal major disadvantages. [1]. This design incorporates a built-in tolerance for process variation, ensuring close static noise margin distribution across all process corners.

The Schmitt Trigger (ST) cell being suggested achieves 1.56 Times higher RSNM than the typical 6T cell. [3]. In order to address all cell VDD-min stability problems for write and read processes, especially read cell current decay, this study recommends using Data-Aware Power-Supplied (D2AP) 8T cells with enhanced bit lines. This cell improves RSNM by 2.9x than 6T SRAM. [4]. The read vs write problem which exist in 6T static random-access memory can be solved by applying Schmitt trigger fundamentals to cross coupled inverter pair. In comparison to the 6T bit-cell (Vcc=300mV), this study offers 58% higher RSNM. The hold static noise margin for 6T and the proposed design are almost identical [5]. This study uses half-selection disturb-free technique to address the disturbance in this state. Sensing interior terminal voltage of an SRAM through a transistor's gate during a read operation is one way to raise RSNM This design's average RSNM outperforms conventional and ST-2 about 2.53 and 1.23 times, respectively. [7]. By Using Fin-FET technology, the RSNM is enhanced and it also has low power consumption. This structure has modest area and read SNM values comparable to 9T cells and higher than 6T cells [9]. This suggested bit-cell uses read buffers to avoid the read-disturb problem and to detach storage nodes from bit line.

Hence, in transistor scaling, read and write processes do not conflict. The mean value of RSNM is improved by 26 percent than traditional 8T static random-access memory [10]. In this paper due to the usage of transmission gate, there is no scalability issue exists between reading and writing process. The SB9T cell outperforms the 6T SRAM cell by 3.9 RSNM at 0.5 V [12].

The proposed cell has 2.77 times RSNM than the standard 6T static random-access memory. With the help of an extra write assist the proposed cell provides 5.14 times more write static noise margin for write '1' than TPDF9T cell [16]. This proposed cell has RSNM which is 83.4 percent greater than 6T SRAM. The WSNM of this cell is 29.5 percent more than 6T static random-access memory [20]. By using cross-coupled inverters write ability is improved. The worst case RSNM for the proposed cell is 94.83 mV [21]. The proposed cell provides enhancement in read stability by using Schmitt trigger inverters. It also provides improvement in write ability by using selective power gating techniques [22]. The proposed cell uses 28.20 percent less power than 6T SRAM. RSNM of this is 10.63 percent more than 6T SRAM cell. Write SNM of this is 33.09 percent more than 6T SRAM cell [23]. In this paper, a 10T static random-access memory cell which is free from half select issue is presented. Proposed cell provides 2.02 times enhancement in RSNM as well as 2.02 times improvement in WSNM than 6T SRAM [25].

2. Access Time (WRITE AND READ):

In order to increase process variation tolerances, this study suggests an ST-based differential bit-cell with a integral feedback mechanism. It enhances 14% more WAT than the 6T cell. It shows 42% higher average RAT than the 6T cell [3]. As word line reaches 50% from its initial low (high) level, T_{RA} is calculated. [6]. This proposed cell has more WAT than other cells. This design uses two transistors in place of using only one unlike other designs for writing path [12]. The RAT of proposed cell can be estimated where the point RD pin increases to Vdd/2 up to the bit line is discharged to Vdd/2. Both RAT and WAT become worse through scaling of supply voltages [24]. RAT of proposed cell is increases with the decrease in supply voltage. This cell gives 1.22 times narrower WAT than 6T SRAM. This cell gives 1.83 times narrower RAT than 6T SRAM [25].

3. Read Stability and Write Ability:

To improve cell stability, this cell uses the sturdy inverter pair. With the help of feedback transistors switching threshold of inverter increases when the node storing bit '1' is discharged to the bit '0' state [3]. In this study, we found that for correct write operation the size of cell must be strong. It also has been examined that in nanoscale technology process variation effect increases. To remove sizing problem, feedback transistors has been used [11]. In this cell, detached read buffer has been used for read process. Read stability as well as hold stability of this cell is like conventional 8T cell. With the help of butterfly curve method read stability is calculated. With the help of write margin write ability is calculated [12].

4. Process Control Variation:

The proposed cell has in built process variation tolerance circuit. Switching threshold voltage of an inverter will increase or decrease based on working of nmos [3]. In this paper SRAM with Schmitt trigger which works in differential mode and can be useful for low voltage operations is presented. In this proposed work, process variation tolerance can be improved with the help of in-built feedback implementation. This proposed cell can be useful in future technologies [5]. In this work, an effort is made to reduce process variation issues in the conventional 6T cell while maintaining its fully differential structure and having minimum area [6]. This paper proposes, advanced Fin-FET based 12T static random-access memory cell (WWL12T). This proposed work gives lesser values of process variation as well as lesser value of SCT [11]. The process corners describe the region of process variations where circuit can operate correctly. For this examination, to have pull up ratio and cell ratio equal to 1 we kept all the transistors size same. From the observation we get WSNM at SF corner is lesser than the WSNM at all other corners [15]. The corner-based method is used in this research to determine how process variation affects circuit performance. The main cause of the first process differences is the manufacture of integrated circuits. The performance of the circuit is impacted by the process variance. [18].

5. Data Retention Voltage (DRV):

The DRV is defined as least amount of supply voltage needed to save the data. The DRV is calculated with the help of DRV of worst-case cell [13]. DRV is estimated by the help of butterfly curve method. In this study dc analysis has been used for DRV calculations. Due to dc analysis DRV from before layout and after layout is similar [14]. In this work, DRV of different SRAM cell has been analysed for different process corners with the changes in temperature and sizing ratio. DRV can be calculated from butterfly curve method. In this study, it is found that that value of DRV is smaller at FF corner and larger at SS corner for lowest temperature [18].

III. LITERATURE REVIEW

In this paper, with the help of CMOS, an analytic expression for static noise margin of SRAM cell is analysed. A quick and easy SNM simulation method has been proposed. It has been discovered that to maintain adequate SNM values at reduced supply voltages, R-load cells require similar or equal area to full-CMOS cells. **[Seevinck E et al. (1987)] [1].** Sub-voltage SRAM circuits presented in this work provide more than two times the speed of typical low voltage static random-access memory. An unexpected flip of the SRAM cell could happen in the DLC SRAM due to the well bias voltage's dynamic fluctuation. **[Hiroshi Kawaguchi et al. (1998)] [2].** The present paper presents a differential 10-transistor static random-access memory that uses Schmitt Triggers (ST) which is suitable for subthreshold operations. This cell provides better static noise margin as well as it can operate at lower V_{DD} than conventional 6T SRAM.

[Jaydeep P. Kulkarni et al. (2007)] [3]. This paper addresses the stability and trade-off issues inherent in traditional 8T and 6T cells. This design enhances write margin, half-selection stability, and read stability for low-V_{DD} applications. An enhanced bit line system is used in the proposed 8T cell to improve read stability and speed. **[Meng-Fan Chang et al. (2010)] [4].**

An ST bit-cell provides improved read and write stability than a typical 6T bit-cell. Schmitt trigger bit-cell SRAM has significantly higher write-trip-point, 120 mV lower read-V_{min} and 1.6 times larger RSNM than the 6T SRAM. **[Jaydeep P. Kulkarni et al. (2011)] [5].** This paper outlines a method for creating an SRAM cell that is aware of variability. This circuit is specifically an attractive option for scaling technologies due to the impact of severe PVT changes. **[A. Islam et al. (2012)] [6].**

An innovative 9T SRAM cell with superior write performance & enhanced read stability has been presented. SRAM with 256-kb capacity uses 37% less area over 6T than SRAM with 9T cells. **[Ghasem Pasandi et al. (2014)] [7].**

This paper introduces an innovative 8T SRAM cell design based on conventional silicon technology. The new cell design has significantly reduced leakage power than the typical SRAM circuit. It addresses the problem of half selection with the proposed new scheme for low-power internal write-back. **[Ghasem Pasandi et al. (2014)] [8].** This paper presents the construction of 7T SRAM cells that are fast and reliable when writing. The 7T cell may be a better design choice since it gives good performance and consumes less power. In all scenarios, this design encounter requisite sigma value. **[Mohammad Ansari et al. (2015)] [9].** A new metric called the SNM per unit area to power delay product ratio (SAPR) has been developed for evaluation of trade-offs between different SRAM cell performance parameters. The proposed cell has the second-best SAPR out of every possible cell configuration. **[Sayeed Ahmad et al. (2016)] [10].** This research proposes a 12T SRAM cell based on modern Fin-FET and self-refreshing logic (WWL12T). It consists of an additional word line and a feedback circuit to accommodate bit interleaving for stable space applications. This cell eliminates read disturb, write half-select disturb, and improves write ability. This cell could be used in space and military applications. **[Nandakishor Yadav et al. (2017)] [11].**

An area-efficient 9T SRAM with small bit lines, low leakage, and a half-select free capability are presented in this paper. This design is compatible with bit interleaved architecture. The suggested cell might work well for low-power, high-throughput tasks that involve a lot of reading. **[Sayeed Ahmad et al. (2017)] [12].**

By using a novel read assistance technique, this design increases the read operation. This cell design offers significant improvements in various performance parameters. **[Shourya Gupta et al. (2017)] [13].** The present paper uses supply read retention voltage and word-line read retention voltage to evaluate the read stability of a 6T SRAM cell. The comparison reveals that the acquired results are nearly identical to and even better than the previous results. **[Dasgupta et al. (2017)] [14].** The suggested research investigates SRAM write stability in the subthreshold region. According to this analysis, the Write stability is worst at the slow-fast (SF) corner. The WSNM is the least in this corner. At the fast-slow (FS) corner of each voltage range, the WSNM is largest. **[Ruchi et al. (2017)] [15].** The suggested 10T SRAM is immune to soft errors because it is capable of bit interleaving. **[Shivram MANSORE et al. (2018)] [16].** This paper proposes two approaches. The simulation results show that using the proposed half-selection techniques considerably reduces the average failure probability. The proposed methodologies also help to reduce power consumption. **[Ghasem Pasandi et al. (2018)] [17].** By analysing the DRV at the process corner, it evaluates the stability of SRAM. DRV is lowest at lower temperatures in the FF process corner and highest in SS process corner. Working with DRV (DRV) values is best done in the fast-fast (FF) region. **[S. Dasgupta et al. (2019)] [18].** This proposed approach employs two voltage sources, one connected to the bit line and the other to the bit bar line, respectively, to avoid the swing voltage at the output nodes of the bit and bit bar lines. Future low-power devices like cellphones, laptops, computers, and other devices could use this model. **[K. Gavaskar et al. (2019)] [19].** This paper describes a new single-ended PPN-based 10T static random-access memory with excellent read stability. The suggested cell's figure of merit (FOM) is 1.513x higher than a 6T SRAM cell and higher than all other cells. This cell is best for systems where energy and performance are the main issues due to its higher figure of merit (FOM). **[Prachi Sanvale et al. (2019)] [20].** This paper proposes 11T SRAM cell powered by its bit line pair. This design cell has 99:97 percent, 99:93 percent, and 99:97 percent leakage power reductions. Furthermore, this design cell has demonstrated its rigidity about half-select issues. **[Vishal Sharma et al. (2019)] [21].** This paper presents ST based 9T SRAM cells having a single bit-line structure that achieve high read stability due to the one-sided Schmitt-trigger inverter. It has improved static noise margin than previously available cells. **[Keonhee Cho et al. (2020)] [22].** The paper presents a variation-tolerant, dependable 11T SRAM structure that can perform successful write/read operations while consuming minimal read power. This system shows stability, is energy efficient, and has a moderate delay. This design consumes the lesser read energy than other topologies. **[Ashish Sachdeva et al. (2020)] [23].**Using ST inverters in the core latch, this ST12T cell tackles the issue of access transistor sizing by improving the RSNM. The suggested bit-cell array allows for bit interleaving and is half select free. **[V. K. Tomar et al. (2020)] [24].**

The proposed takes advantage of the improved write operation provided by loop-cutting transistors while reducing read power through a decoupled read operation. The proposed cell improves WSNM by 14.94 percent and RSNM by 2.02 times more than the typical 6T SRAM. The proposed cell has the value of the read-current to bit-line leakage current ratio is 2.75X more than the typical 6T SRAM cell. **[Vinay Tomar et al. (2021)] [25].**

IV. COMPARISION OF PERFORMANCE PARAMETER

It is necessary to understand the power, area, and latency characteristics of SRAM for memory applications. In comparison to other SRAM cells like the 6T, NC, and 8T, the suggested cell has the benefits of a smaller area and less power dissipation. The suggested cell provides reduced parasitic capacitance because there are fewer transistors, which decreases the delay. One of the biggest challenges is to reduce the area while maintaining fast speed and low power loss. With the help of the Butterfly and N-curve method stability (SNM) of SRAM is calculated. Since it lacks a perfect discharge path, its noise margin is lower than that of a 6T cell. [26].

The SE6T SRAM cell uses only one bit-line for write and one bit-line for a read. In contrast to conventional 6-T SRAM cells, it consumes only 50% less power. Heterogeneous SRAM cell has been suggested for the embedded memories using multimedia applications. Comparing this design to 6T SRAM cells, this has a small area and power penalty compared to SRAM cells with a 6T Bit Error Rate. By evaluating dynamic power, leakage power, and area required to achieve a given PSNR, the proposed SRAM cell outperforms the conventional 6-T SRAM cell [28].

The below shown Figure IV.1 is the schematic of standard 6T SRAM cell.

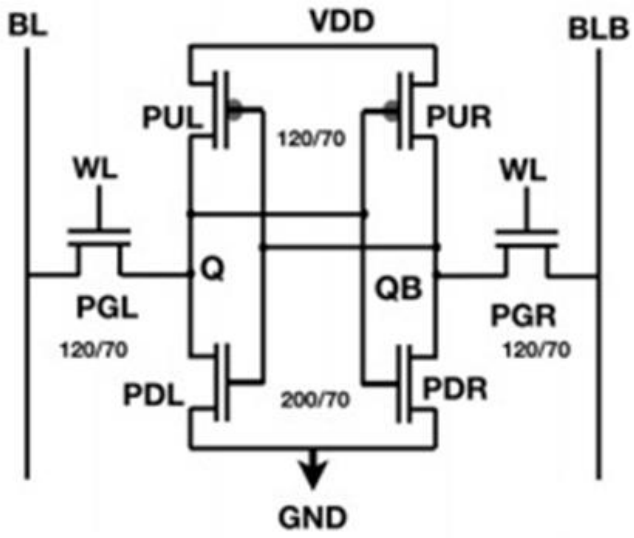

Figure IV.1 Schematic of Standard 6T SRAM [28]

A. Summary Table

Below shown is the Table for comparison of different performance parameters of SRAMs (Starting 10 Papers from literature review) as well as the Summary Bar Graph of complete literature review.

Author's Name and Year	Wsnm &Rsnm	Wat & Rat	DRV	Write And Read Stability	Process Control
Seevinck E et al. (1987)	Improved	-	-		
Hiroshi et al. (1998)	-	-	-	-	-
Jaydeep et al. (2007)	-	Improved	-	Better	Improved
Meng-Fan et al. (2010)	Higher	Improved	-	-	-
Jaydeep et al. (2011)	Higher	Improved	-	-	Built in feedback
A. Islam et al. (2012)	1.3x	1.1x & 1.3x	-	-	Access TG
Ghasem et al. (2014)	Improved	Improved	-	-	-
Mohammad et al. (2015)	Extra Transistor	-	-	-	-
Sayeed et al. (2016)	Improved & Minimum				
Nandakishor et al. (2017)	6.4% Improved	-	-	Self-refreshing node	Less

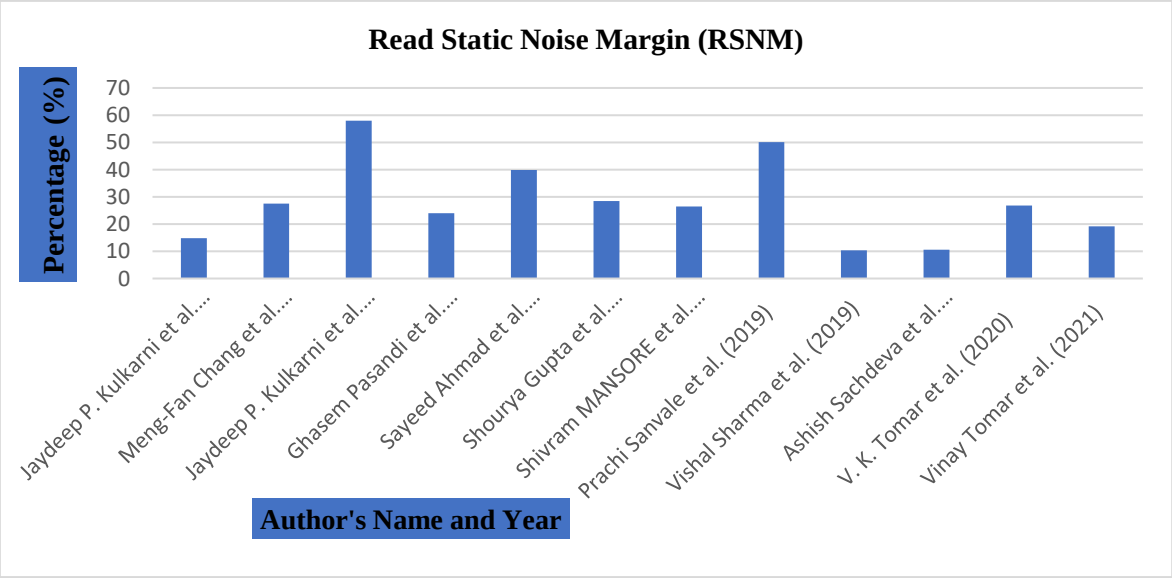

Figure IV.2 Rsnm of 6t Sram (Literature Review)

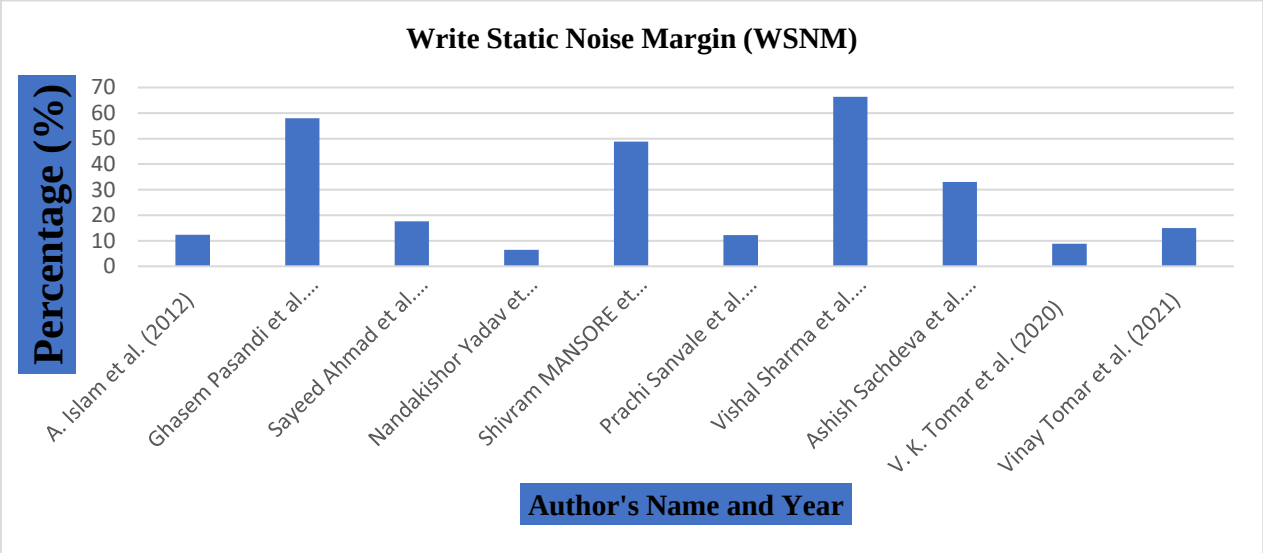

Figure IV.3 Wsnm of 6t Sram (Literature Review)

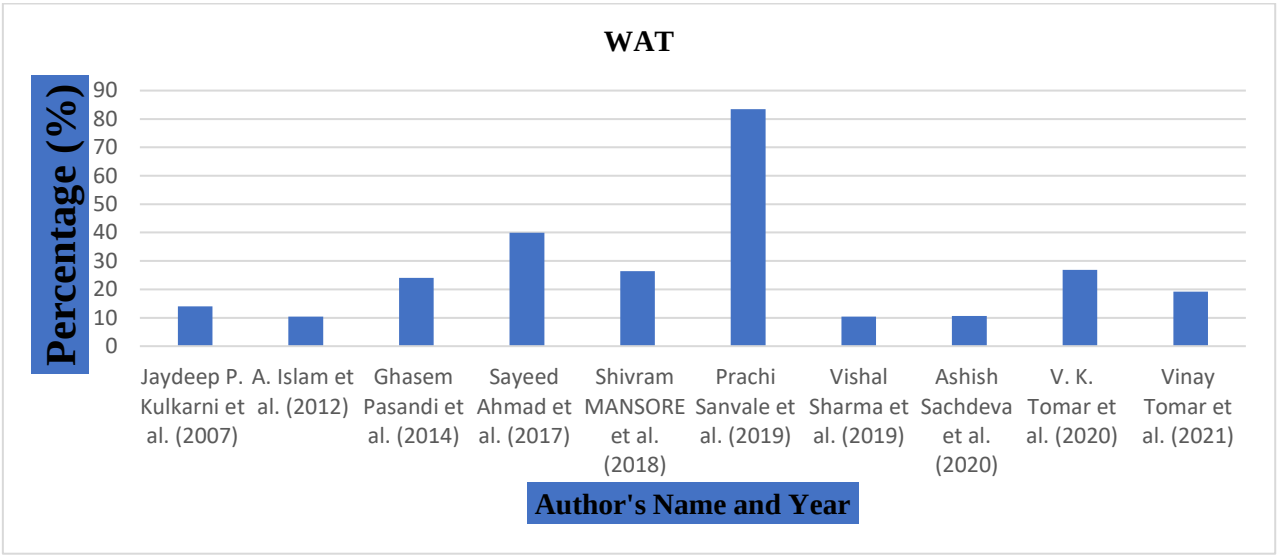

Figure IV.4 Wat of 6t Sram (Literature Review)

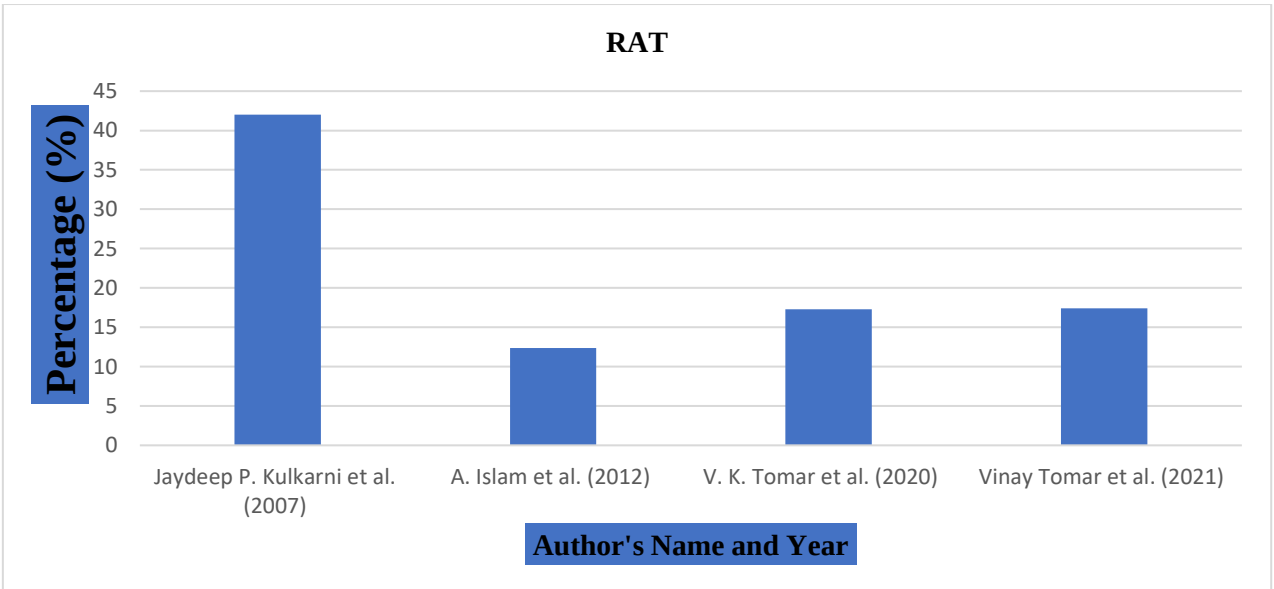

Figure IV.5 Rat of 6t Sram (Literature Review)

V. RESULT AND DISCUSSION

For applications that uses images and videos for the processing of the data, the memory embedded in the system uses a lot of energy. A review of the existing architecture is discussed in this review paper. For memory applications, it is essential to comprehend the power, space, and latency properties of SRAM. The suggested cell has advantages over SRAM cells such the 6T, NC, and 8T including a smaller space and less power dissipation. Because there are fewer transistors in the recommended cell, the parasitic capacitance is minimized, reducing the delay. Keeping up speed and low power loss while reducing the area is one of the toughest hurdles. In the future, we would like to expand on this outline to include applications for IOTs, biomedical technology, and energy harvesting.

DECLARATION

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Authors Contributions	All authors have equal participation in this article

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