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Low Power Embedded SoC Design

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Abstract: ***Now a days all embedded processors are manufactured in such a way that it may consume low power to provide longer life to the system using various low power techniques like clock gating, data gating, variable frequency mechanism, variable voltage mechanism and variable threshold techniques. In this paper these techniques are implemented using VHDL language in Vivado and results are compared to identify the better one among all possible ones. There are various characteristics compared here are power consumption, number of look up tables and number of flip flops consumed.***

Keywords: VHDL, Clock Gating, Data Gating, Frequency Scaling.

I. INTRODUCTION

Low power enables longer life, so that all processors should be designed so that it will consume less power. Lower the power consumption lower the heat dissipation and hence the life time of the device is to be increased. Moreover, the systems with latest state of art comes in miniaturization and these low power techniques helps a lot in designing embedded processors.

II. LITERATURE REVIEW

Himanshu Chaudhary et al [1] explained the need of reducing power consumption especially in the area of synchronous design where the clock usage is high. With the use of clock gating technique, the power consumption was greatly reduced. V. Keerthana and Prasanth. J [2] demonstrated that in how many ways we can optimize the clock gating in order to reduce the power consumption by greater level. Priya Singh and Ravi Goel [3] explained briefly about the power optimization technique in sequential circuits using clock gating technique in order to reduce the power consumption and for better design of the system.
Dushyant Kumar Sharma [4] realized that there are some effects on design of the system, if we are using clock gating technique and it is clearly demonstrated.
Saurabh Kshirsagar and Dr. M B Mali [5] explained that clock gating is widely used in low power application to enable power efficient design and it helps to increase the life time of the device. Nandita Srinivasana et al [6] explained the various clock gating techniques in order to reduce the power consumption. Jagrit Kathuria et al [7] demonstrated the review of various clock gating techniques in which we can choose the best technique as per our requirement according to the situation. S.V. Lakshmi et al [8] compared the performance of various clock gating techniques and by that they suggesting which technique is better for which one. Harpreet Singh and Dr. Sukhwinder Singh [9] explained clock gating technique how it reduces the power consumption especially in VLSI circuits. M. Srialatha and G. Shyam Kishore [10] demonstrated that a comparative analysis of look ahead technique in clock gating. It clearly explains the need of low power consumption especially in miniaturization of circuits.
ShmuelWimer et al [11] explained design flow for Flip Flop using clock gating in the era of data driven mechanism in digital circuits. S.C Brunet et al [12] introduces multi clock domain for various circuits which are runs at various speed for optimizing the power consumption. W. Dobberpuhl et al [13] realized that a dual issue CMOS microprocessor for reducing power consumption. Frank Emnett et al [14] introduces the reduction of power usage with the help of clock gating technique. Gary K. Yeap et al [15] realized low power design for digital circuits. Finally, we are generating this paper with 4 sections. Section [1] is giving introduction and clear idea about topic. Section [2] covers literature survey. Section [3] covers basic block diagram. Section [4] covers methodology followed here to generate messages to alert the doctor and tables related to software logic. Section [5] covers results and analysis. Section [6] references.

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III. BLOCK DIAGRAM

Clock gating:

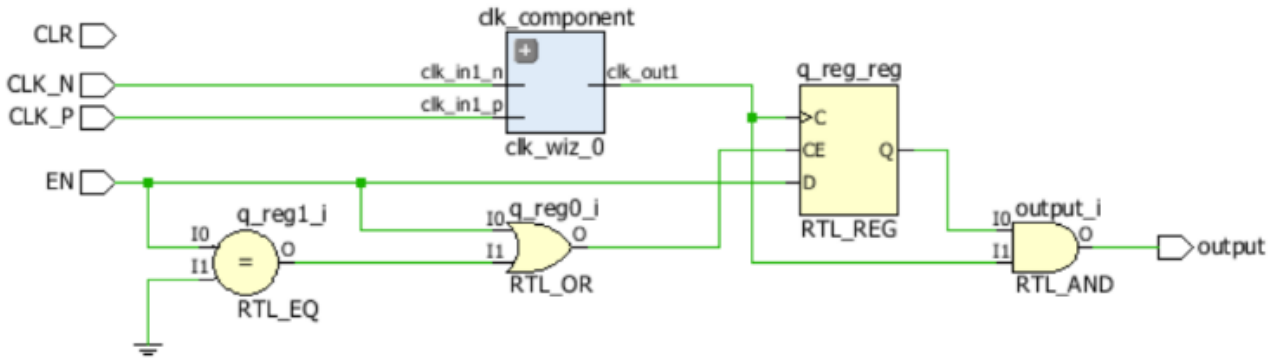

Fig. 1: Clock Gating

The clock gating purpose is to stop the clock when there is no data toggling so that the power may be saved. Here the clock is fed to AND gate, if there is change in data then only output of AND gate is available and it is nothing but gated clock.

Data gating:

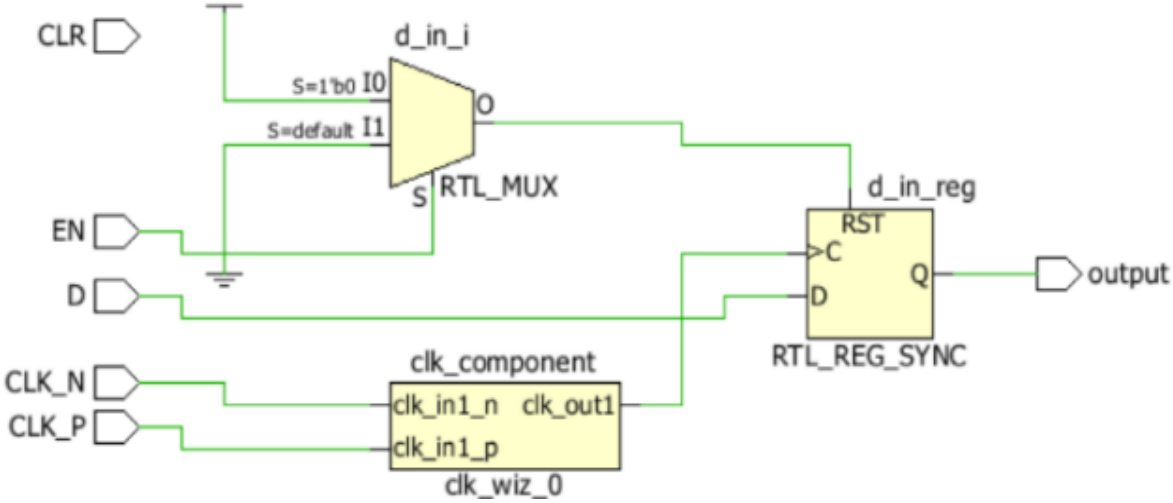

Fig. 2: Data Gating

When enable is equals to zero then there is no change in output otherwise the D may be the output.

Variable frequency:

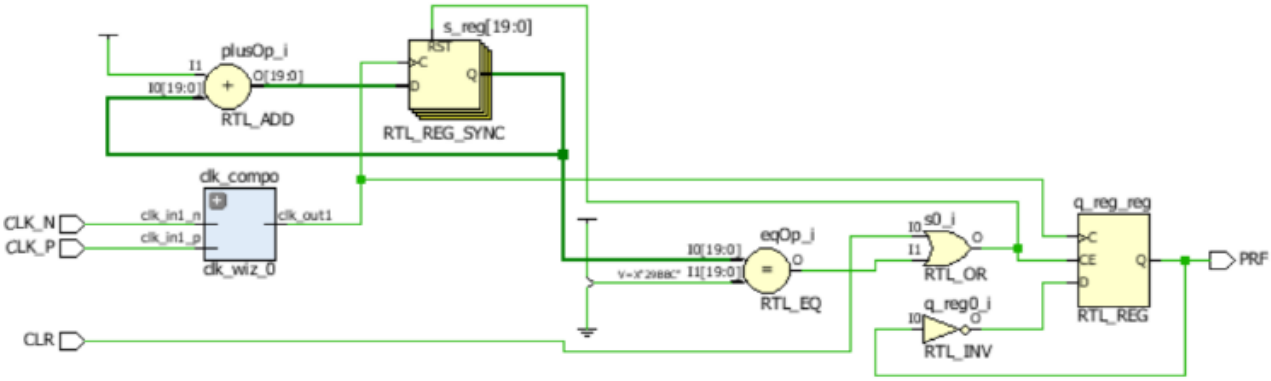

Fig. 3: Variable Frequency

Lower the frequency lower the power consumption. So, the available clock frequency will be scaled to produce the frequencies. For slow speed devices low power frequency may extend whereas high-speed devices will be fed with high clock frequency.

IV. METHODOLOGY

Clock gating:

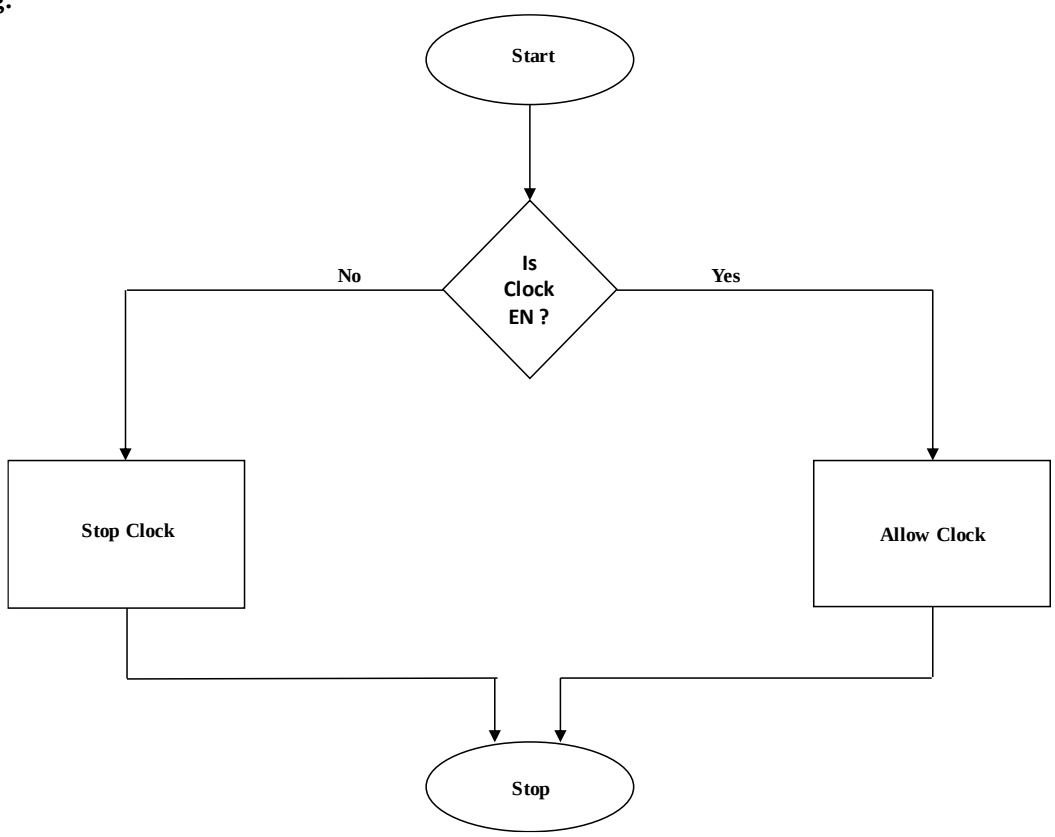

Fig. 4: Flow Chart for Clock Gating

If clock was enabled then it will be allowed further otherwise it will be stopped. If no clock then no power consumption. Clock will be extended based on our requirement so that the power consumption was reduced.

Data gating:

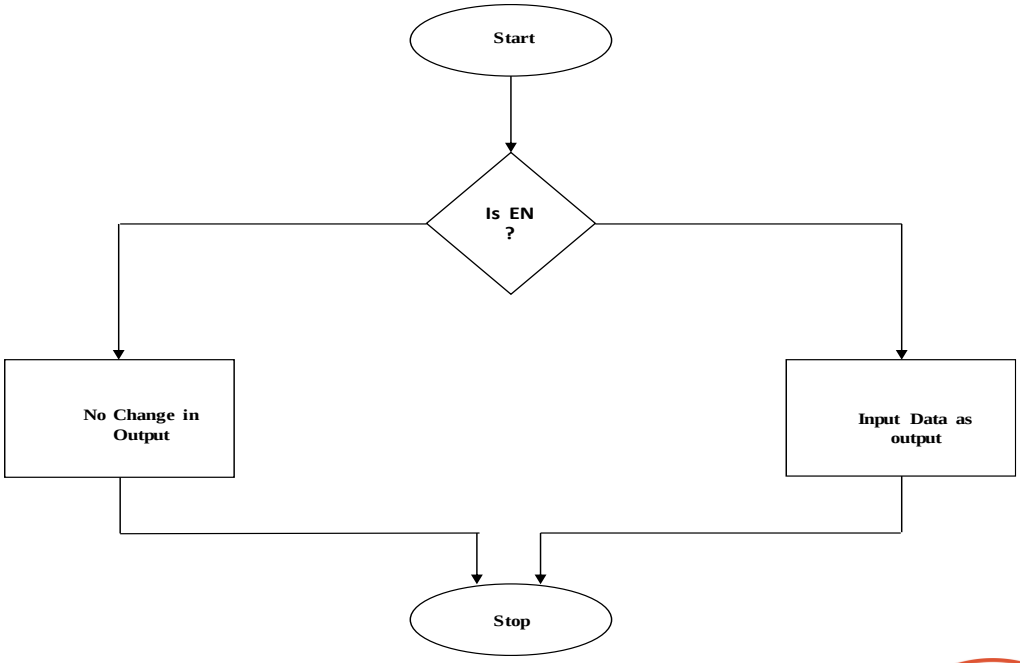

Fig. 5: Flow Chart for Data Gating

If Enable bit is set then only there is change in output otherwise same as previous.

Variable Frequency:

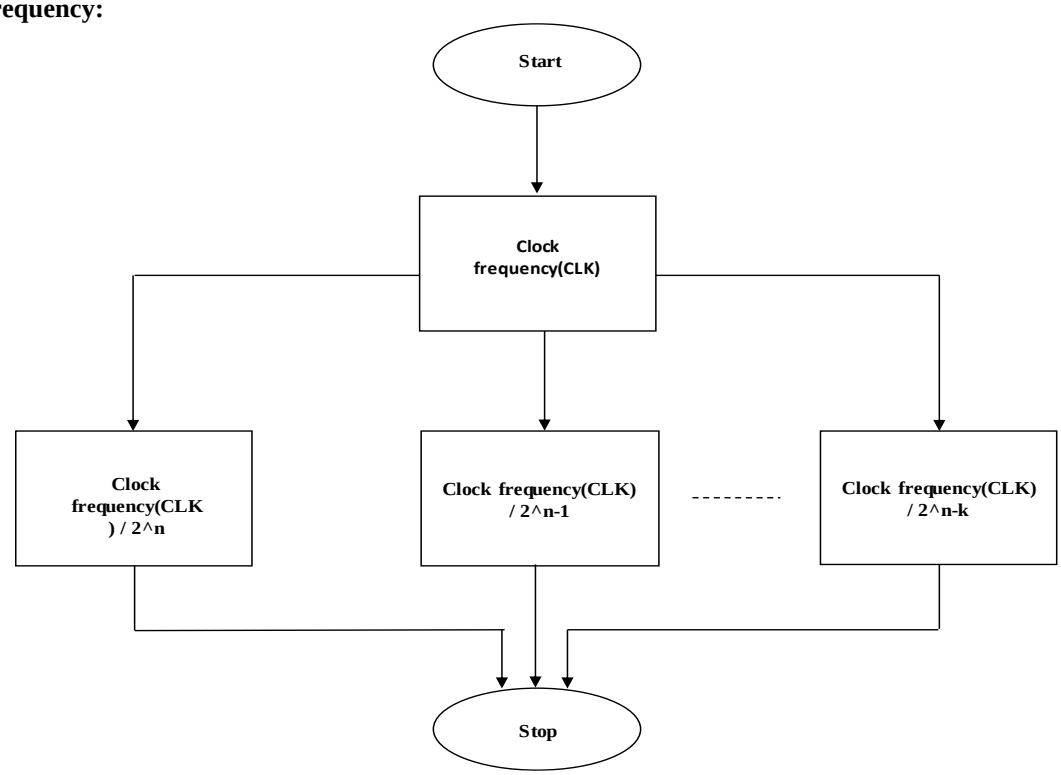

Fig. 6: Flow Chart for Variable Frequency

The clock frequency is divided using counter to get the desired frequency. Lower the frequency lower the power consumption but system also work get slow down. So, the user can go for optimization based on his requirements he may choose the desired frequency accordingly.

V. RESULT AND ANALYSIS

Clock gating:

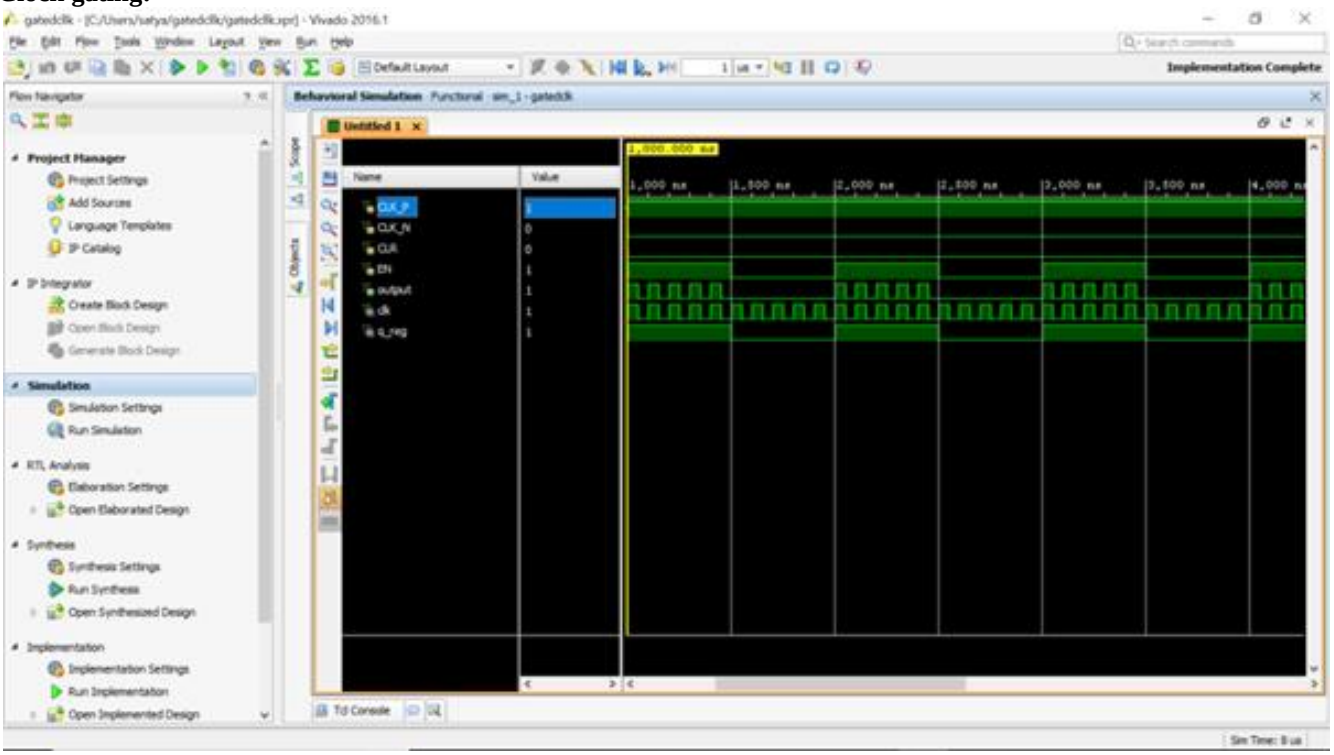

Fig. 7: Waveform for Clock Gating

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The above figure shows the result of clock gating technique. By allowing clock at required duration will help greatly in reduction of power consumption.

Data gating:

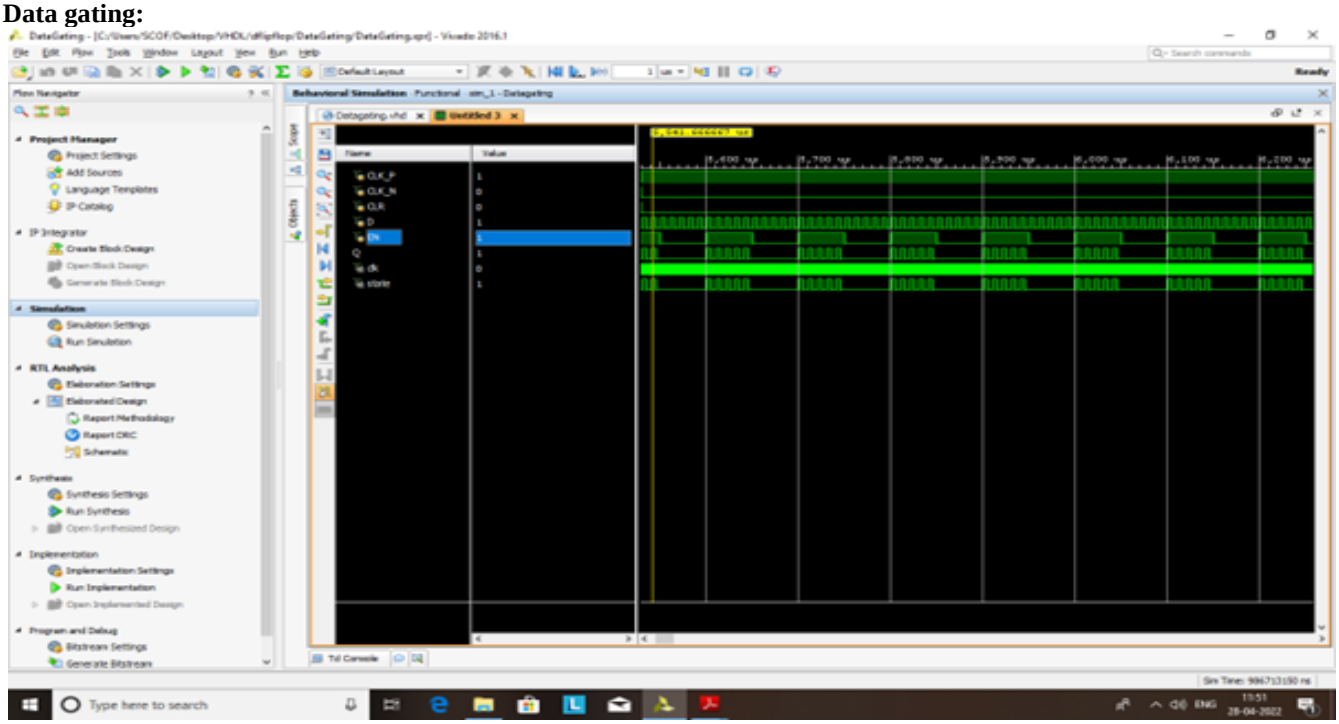

Fig. 8: Waveform for Data Gating

The above figure shows the result of data gating technique. With the help of enable bit we can made the system as active and it leads to reduce the power consumption. Always the result shows data gating is more effective compared to clock gating especially from power consumption point of view

Variable frequency:

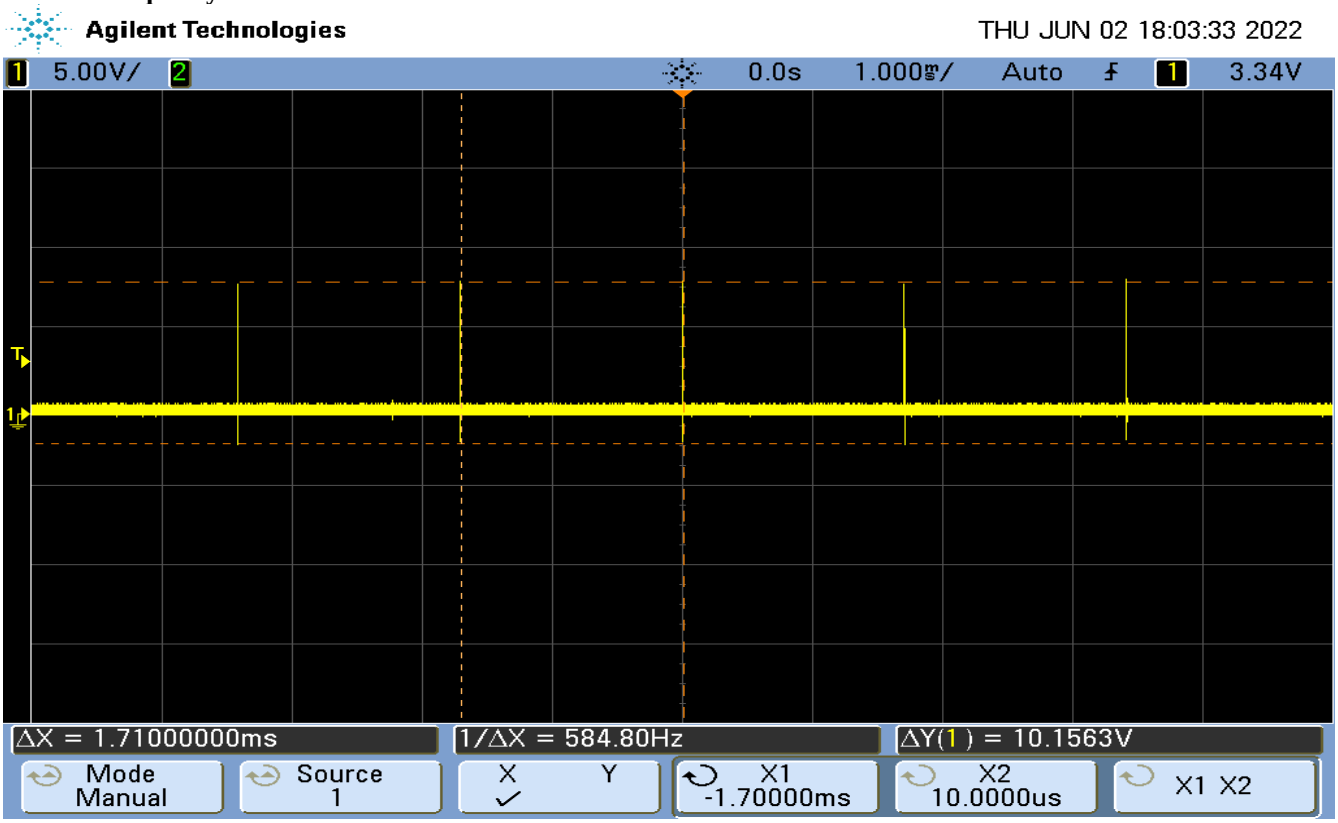

Fig. 9: Output 585 Hz in CRO

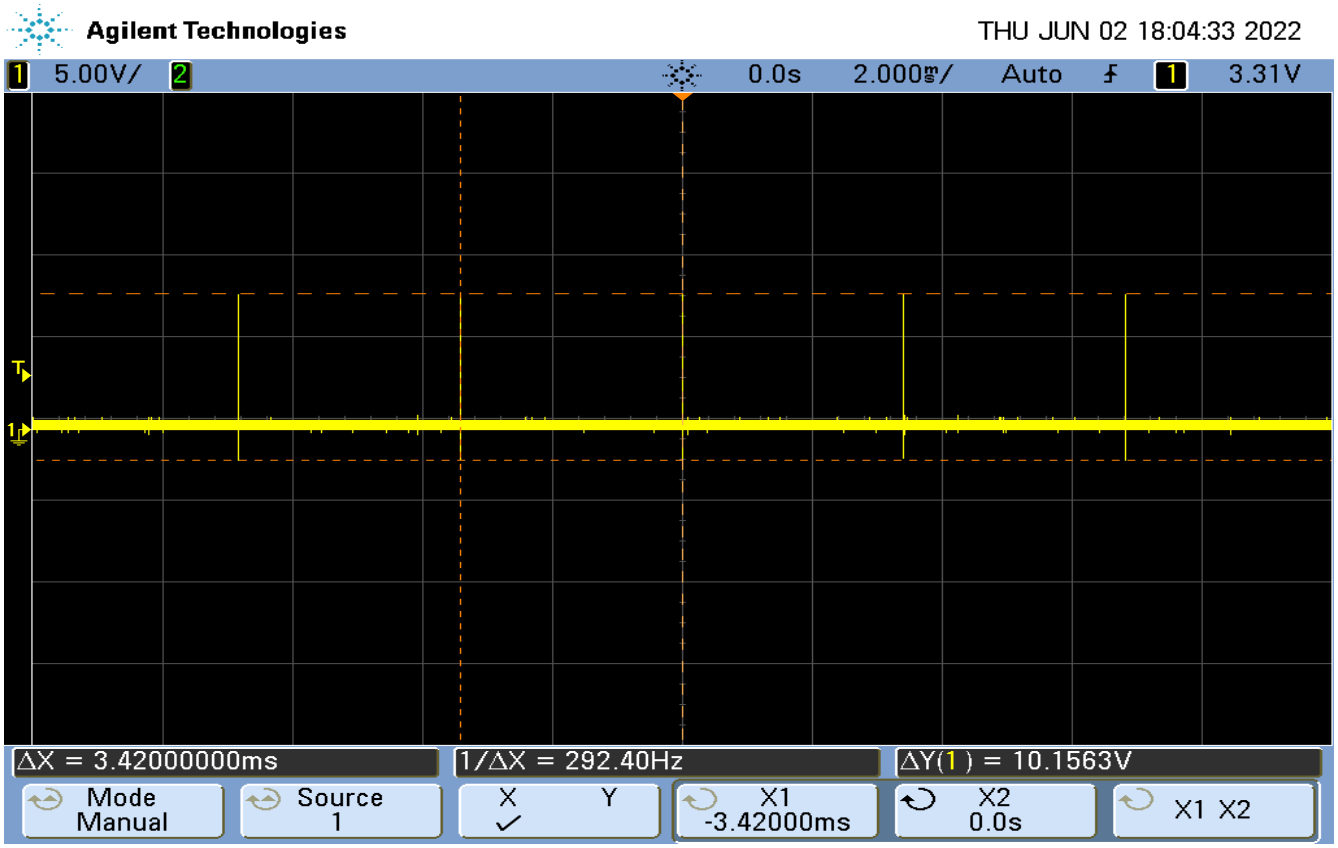

Fig. 10: Output 292 Hz in CRO

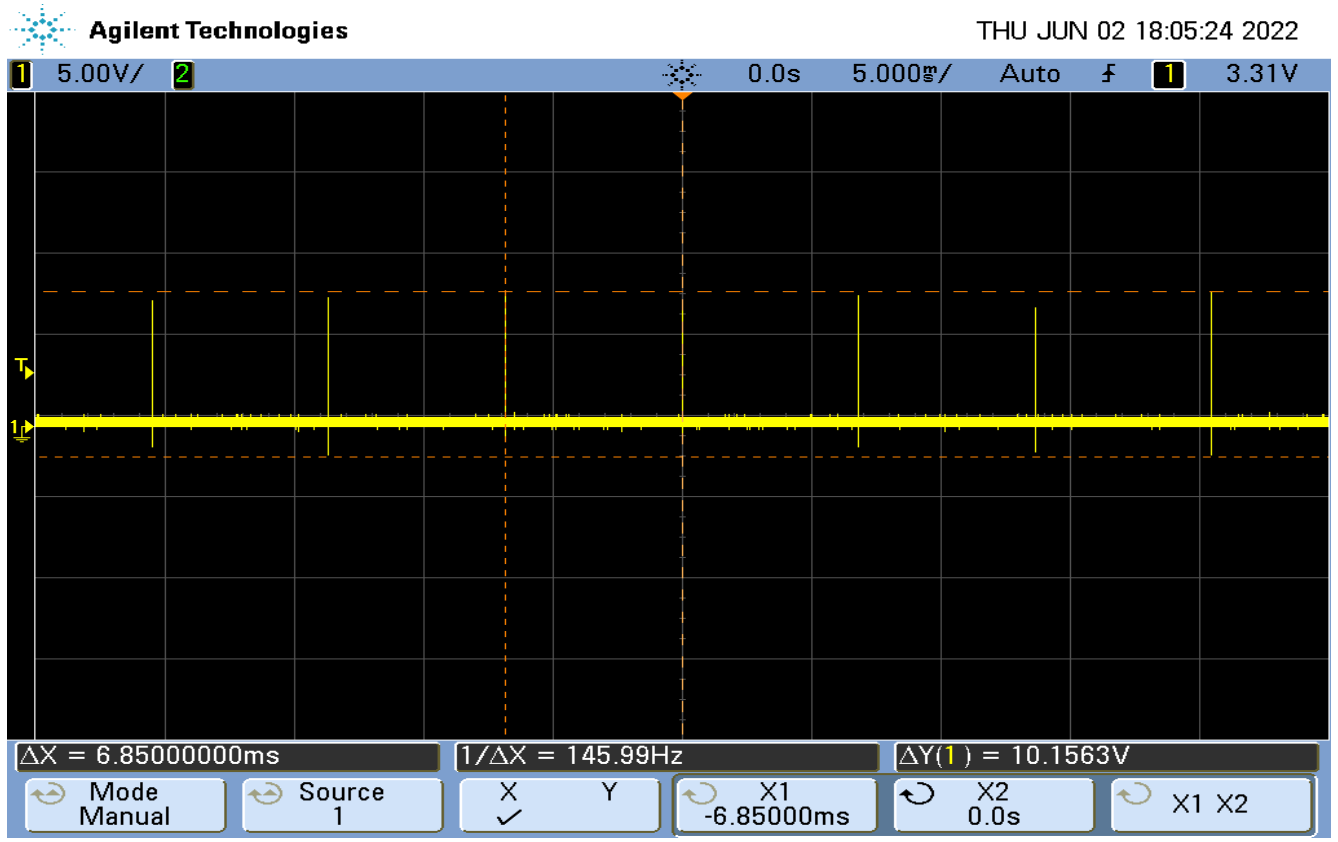

Fig. 11: Output 146 Hz in CRO

The Above three figure shows how to scale the clock frequency using counter. Lower the frequency lower the power consumption.

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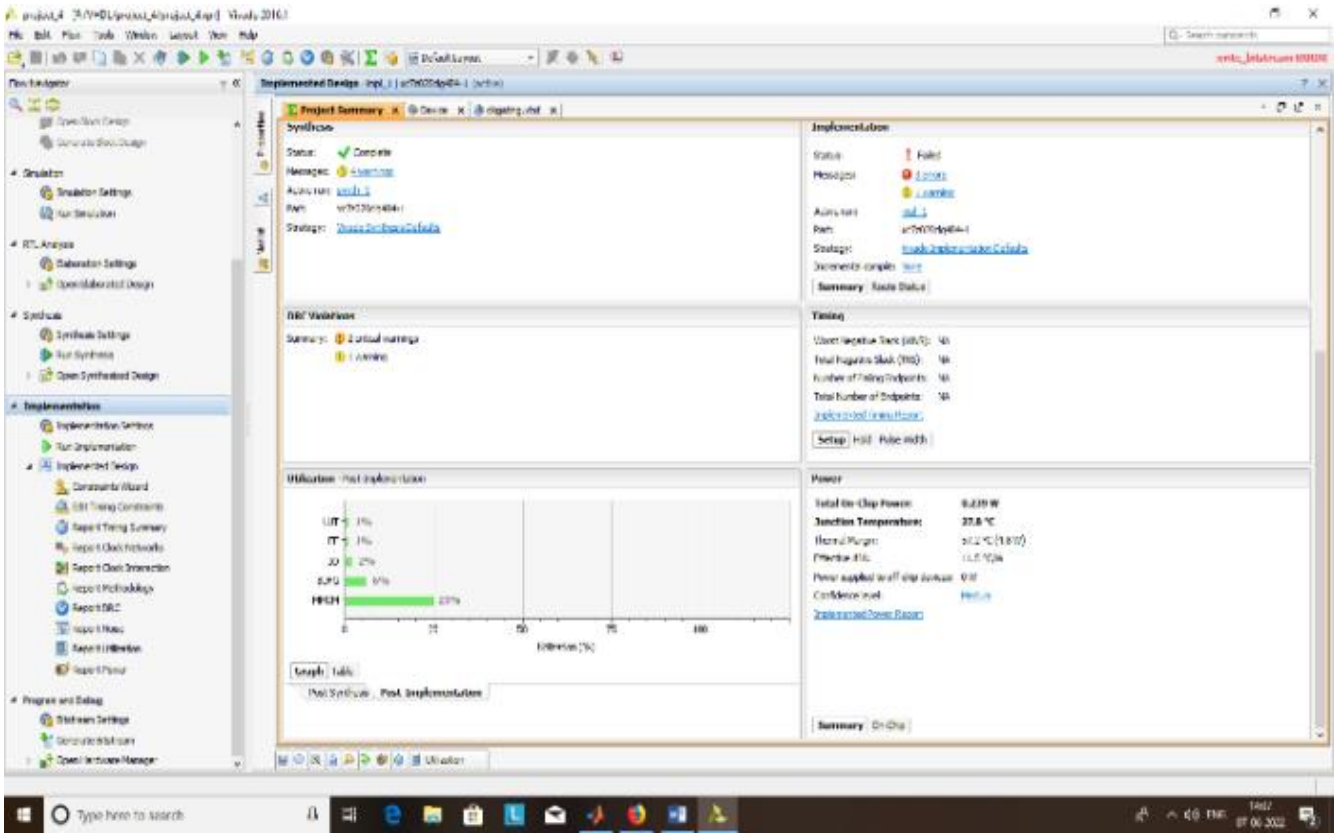


Fig. 12: Clock gating summary

The above figure shows the clock gating summary.it gives the details about power consumption, Look up table, Flip flops, Buffer's, I/O's and memory consumption in percentages.

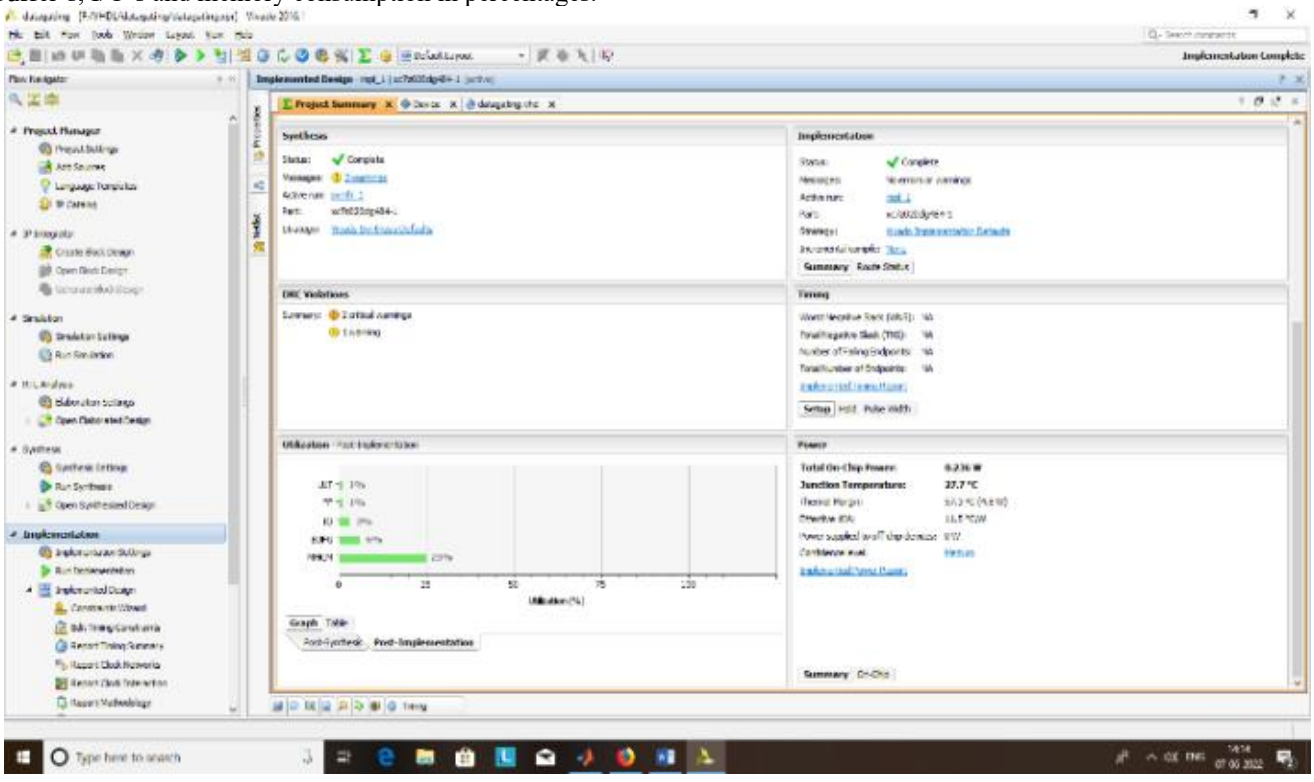


Fig. 13: Data gating summary

The above figure shows the data gating summary.it gives the details about power consumption, Look up table, Flip flops, Buffer's, I/O's and memory consumption in percentages

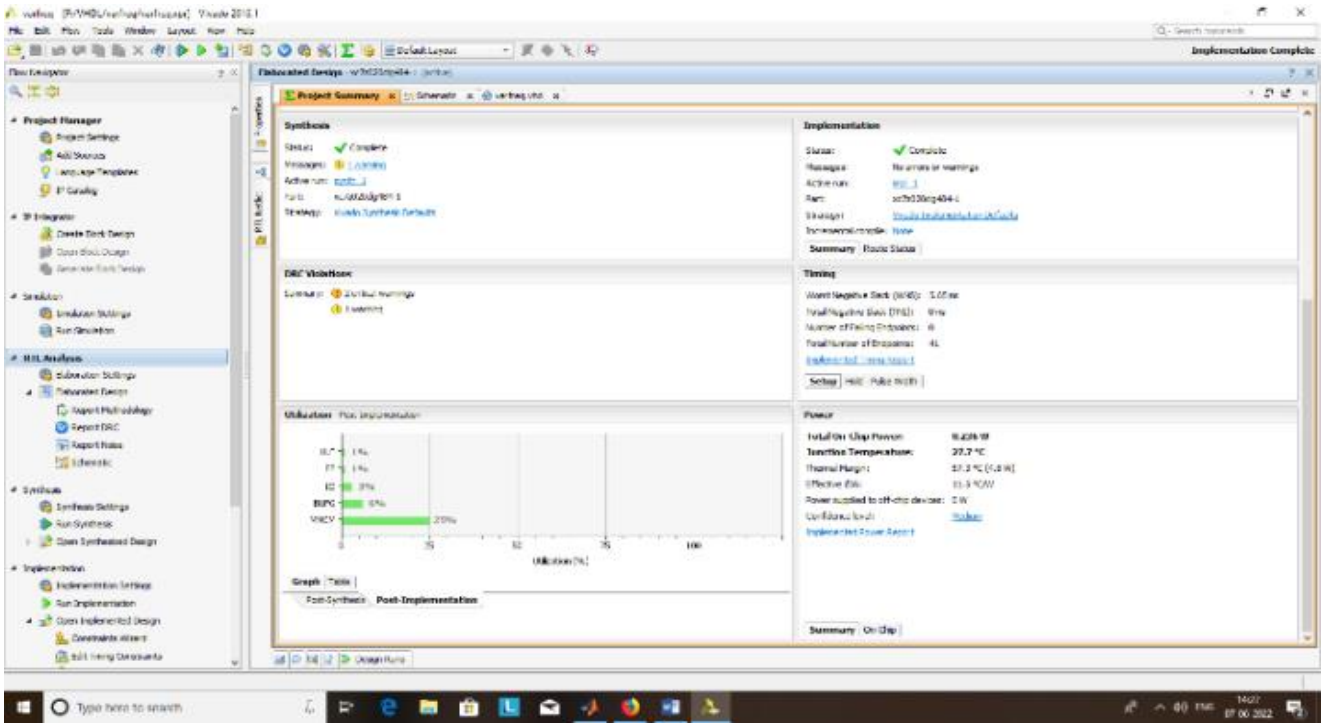
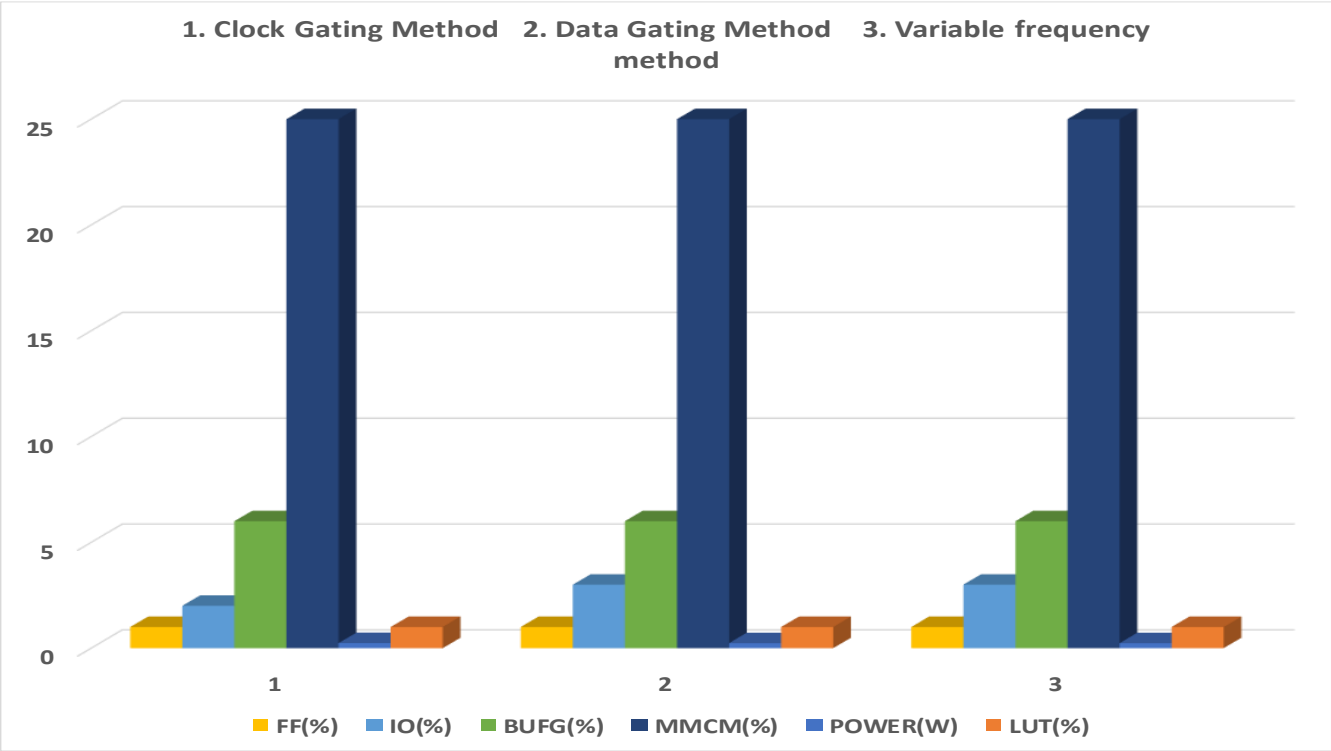


Fig. 14: Variable frequency summary

The above figure shows the Variable frequency summary.it gives the details about power consumption, Look up table, Flip flops, Buffer's, I/O's and memory consumption in percentages

Table 1: Table for Comparison of Parameters using Various Methods

Total On chip Power	LUT %	FF %	IO %	BUFG %	MMCM %	Method
0.239 W	1	1	2	6	25	Clock gating
0.236 W	1	1	3	6	25	Data gating
0.236 W	1	1	3	6	25	Variable frequency



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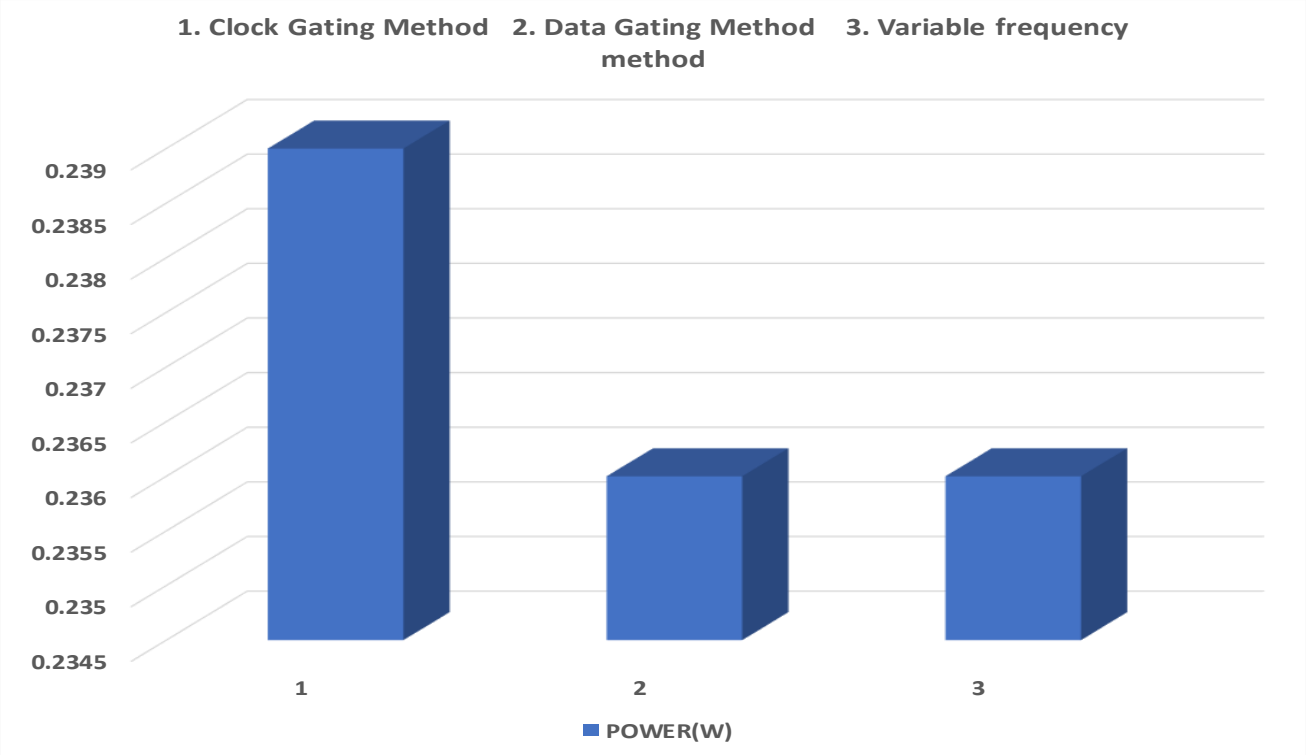

Fig15: Bar graph for comparison of parameters using various methods

VI. CONCLUSION

In this paper, as per results observed by simulation data gating saves more power compared to clock gating. Data gating and variable frequency methods the power consumption was same. Lower the power consumption that leads to lower the heat dissipation and it enable longer life to the system especially in the field of system on chip using Nano meter technology because heat dissipation takes place major role in deciding life time of the device.

DECLARATION

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Conflicts of Interest/ Competing Interests	No conflicts of interest to the best of our knowledge.
Ethical Approval and Consent to Participate	No, the article does not require ethical approval and consent to participate with evidence.
Availability of Data and Material/ Data Access Statement	Not relevant.
Authors Contributions	All authors have equal participation in this article.

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