Indian Journal of VLSI Design (IJVLSID)
ISSN: 2582-8843 (Online), Volume-2 Issue-2, September 2022

Low Power ALU using Wave Shaping Diode Adiabatic Logic

Ishita Khindria, Kashika Hingorani, Vandana Niranjan

Abstract: ***The evolution of portable electronic devices and their widespread application has led to an increased focus on power dissipation as one of the critical parameters. An increase in functionality requirement and design complexity on a single chip has resulted in increased power dissipation. High power dissipation has motivated study and innovation on low power circuit design techniques. Adiabatic logic has been studied as one of the design techniques to reduce power dissipation by reusing the power that was getting dissipated in conventional designs. This paper presents the application of Wave Shaping Diode Adiabatic Logic (WSDAL) to implement an ALU and analyse the improvement in power dissipation as compared to the conventional CMOS design. The WSDAL design uses a slow and time-fluctuating 2-phase sinusoidal Power Clock (PC), which supplies power as well as a clock to the designs. WSDAL uses an Ultra-Low Power Diode (ULPD) structure that operates as a wave shaping device and reduces glitches at the output. The design has been implemented in OrCAD Capture and simulated using Pspice in TSMC 180nm technology. The simulations were performed at 200MHz PC frequency and power dissipation was studied over a range of voltages from 1.4V to 2.2V. The simulations show that WSDAL ALU dissipates less power than the CMOS design. This study indicates that WSDAL-based designs have the potential to be deployed for power dissipation reduction in portable devices.***

Keywords**: *Adiabatic, ALU, Low Power Design, WSDAL.***

I. INTRODUCTION

The advancement in VLSI technology has given rise to an increase in the speed and complexity of silicon chips. This has been accompanied by high power dissipation which is a challenge for mobile electronic devices. It is essential to minimize the overall power consumption in such devices to improve the battery life. To optimize the power consumption, CMOS circuits have evolved by adapting several innovative design techniques. Adiabatic switching is one such low-power technique that has been studied across various designs and applications [1]. The power dissipation is reduced by recovering the energy instead of allowing it to get dissipated as in conventional designs. Several techniques related to adiabatic logic have been studied in the past. Wave Shaping Diode Adiabatic Logic (WSDAL) is an adiabatic switching technique that was recently proposed in [2].

In this paper, the WSDAL technique has been used to implement a 1-bit Arithmetic Logic Unit. The Arithmetic Logic Unit, commonly known as ALU, is a combinational circuit that performs mathematical and logical operations on its inputs. These can be arithmetic operations like add, subtract, multiply or divide and logical or bitwise operations like AND, OR, NOR, XOR, NOT, etc. The components of 1-bit ALU including Inverter, Half Adder, AND gate, NOR gate, XOR gate, and 4:1 MUX have been implemented using the WSDAL technique in OrCAD Capture. The power dissipation in all the circuits has been compared with conventional CMOS-based ALU by performing Pspice simulations in TSMC 180nm technology.

II. ADIABATIC LOGIC

In CMOS designs, power dissipation consists of mainly three components: static, dynamic, and short-circuit power dissipation. In static power dissipation, the output of the circuit is in a steady state of logic ‘0’ or ‘1’. It is also called steady-state power dissipation as there is no switching activity that takes place in the circuit. Leakage current is the reason for static power dissipation in CMOS circuits. This leakage current is mainly composed of subthreshold leakage and reverse-bias diode leakage current. The value of static power dissipation in a CMOS circuit is given by (1) [3]:

$$P_{static} = I_{static} V_{DD} \quad (1)$$

Where I_{static} is the current flowing through the circuit when it is in a steady state with V_{DD} as power supply. The short-circuit between the supply voltage, V_{DD}, and ground causes short-circuit power dissipation. While the switching activity is taking place, at some point, the nMOS as well as pMOS device, will be ON. This will create a short circuit between V_{DD} and the ground because of which huge currents will flow causing large power dissipation. Many methods have been devised to ensure that short-circuit power dissipation is much less than the dynamic power dissipation by at least 20 percent. This can be done by ensuring that input rise/fall time and output rise/fall times are equal [4,5]. Charging and discharging of the load capacitor causes dynamic power dissipation that takes place during the transient phase in the CMOS circuits. In conventional full output swing, the energy drawn through the power supply during charging of the capacitor is $C_{load}V_{DD}^2$. The amount of energy in the capacitor after fully charging is $1/2C_{load}V_{DD}^2$.

Manuscript received on 16 July 2022 | Revised Manuscript received on 23 July 2022 | Manuscript Accepted on 15 September 2022 | Manuscript published on 30 September 2022.
***** Correspondence Author
Ishita Khindria*, Department of Electronics and Communications, Indira Gandhi Delhi Technical University for Women, Delhi, India. Email: ikhindria@gmail.com
Kashika Hingorani, Department of Electronics and Communications, Indira Gandhi Delhi Technical University for Women, Delhi, India. Email: kashika2212@gmail.com
Vandana Niranjan, Department of Electronics and Communications, Indira Gandhi Delhi Technical University for Women, Delhi, India. Email: vandana_niranjan@yahoo.com

The rest of the energy is dissipated across the pull-up network transistors. While discharging the load capacitor, the $1/2C_{load}V_{DD}^2$ energy stored in the capacitor is dissipated across the pull-down network. This is the main component of power dissipation in CMOS. It can be reduced to some extent by decreasing the load capacitance or reducing the supply voltage. To further minimize this dissipation of power, a part of the energy drawn from the power supply can be used more effectively by reusing it [6,7]. Thus, adiabatic logic circuits are being used over conventional CMOS circuits. Adiabatic logic substitutes the generally used square-wave clock with a slow and time-fluctuating Power Clock (PC), which supplies power as well as a clock to the designs. Adiabatic designs typically need multiple clock phases to work accurately. The widely recognized kinds of power clocks utilized in adiabatic designs are 4-phase trapezoidal and 2-phase sinusoidal [8]. Adiabatic designs function through charging the node capacitance for some portion of the clock duration, permitting to sample the output at the following clock cycle, and at that point, the charge is recovered from the node capacitance. The power clocks to be used in a circuit relies upon the type of adiabatic logic as well as the oscillator used in the design. In most designs, trapezoidal PCs utilize 4 stages, but some designs that have a single phase and some that have 8 phases. The four phases of trapezoidal power clocks are Wait, Charge, Hold and Recover. Two stages are ordinarily utilized in sinusoidal power clocks; however, a few techniques have extra circuits to accomplish single-phase operation. The two phases that sinusoidal PCs work in are: Charge and Recover. [8]. In the literature, various adiabatic techniques have been reported. ECRL uses pMOS transistors that are cross-coupled [9]. PFAL uses cross-coupled inverters which form a latch [10]. PAL uses pass transistor blocks as well as a two-phase PC [11]. 2PADL uses gate overdrive and reduced switching power [12]. It uses a sinusoidal power clock with two phases and has a single rail output which removes signal routing problems. One of the recent techniques studied in this paper, WSDAL, is based on Ultra Low Power Diode in the CMOS circuits [2].

A. WSDAL

WSDAL uses an Ultra-Low Power Diode structure (ULPD) proposed by [13]. ULPD operates as a wave shaping device and decreases glitches and oscillations at the output as compared to 2PADL and decreases power dissipation.

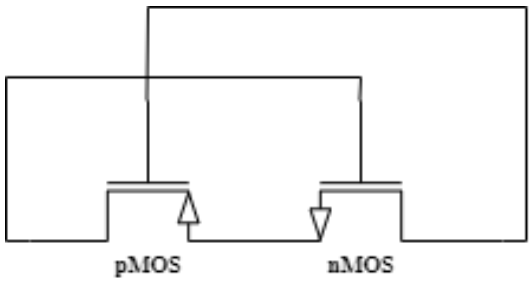


Fig. 1: ULPD Structure

The ULPD structure is shown in Fig. 1 which includes an nMOS and a pMOS device. When the source of nMOS is at low and the drain of pMOS is at a high voltage, then both the transistors will be switched ON and work as an ultra-low power diode and the current will flow in the forward direction. If any of the transistors is OFF then this structure will work as a reverse-biased diode and there will be no current flowing in any direction. The WSDAL inverter designed by using a modified adiabatic technique is shown in Fig. 2 and the output waveform at 200MHz is shown in Fig. 3. In this design, two complementary sinusoidal power supply PC and PCB are used. Transistors M1 and M2 are pMOS while transistors M3-M5 are nMOS. The transistors M2 and M3 form a ULPD. When the input is low and PC is high, then M1 will be ON and M4 will be OFF. Since M1 is ON, M3 will be ON as a high PC value is passed to the gate of M3. Since the output was initially low, M2 will be ON. Thus, the output follows a high PC value. When the input is high and PC is also high, then M4 is ON and M1 will be OFF. M6 is also ON since output was previously high. Due to the voltage difference between the output and PCB, output will get discharged. PCB is used to recover the charge stored here in an adiabatic manner. Whenever PC is low and PCB is high, M3 will be OFF. Therefore, the ULPD acts in reverse bias mode, and the output will retain the previous value. In the simulation results, the first waveform shows two complementary sinusoidal curves PC and PCB, the second waveform shows the input and the third waveform shows the output of the WSDAL inverter.

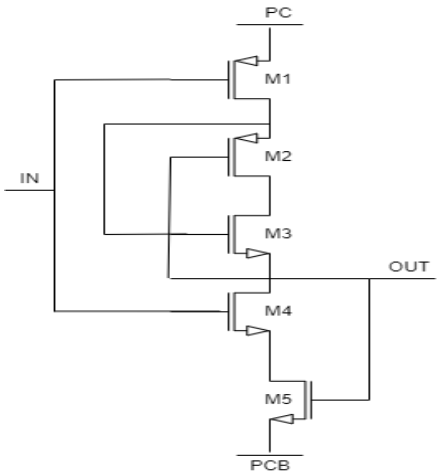


Fig. 2. WSDAL Inverter

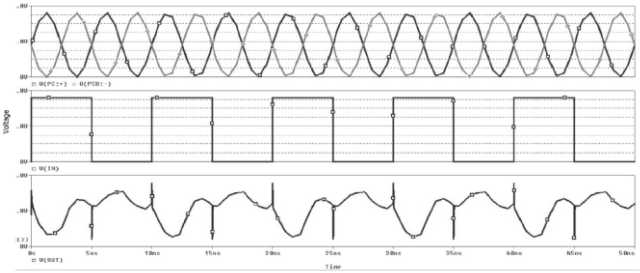


Fig. 3. Simulation Results of WSDAL Inverter

III. PROPOSED WSDAL ALU CIRCUIT

The ALU has been designed to perform four operations: addition, AND, NOR, and XOR on two 1-bit operands. The four operations can be selected through a 4:1 MUX.

The block diagram of the ALU is shown in Fig. 4. The 4:1 MUX is realised using a combination of 3-input AND gates and a 4-input OR gate. WSDAL technique has been applied across all the components of the ALU. The schematic of the ALU is shown in Fig. 5 and its simulation results are shown in Fig. 6. In the simulation results, the first two waveforms indicate the value of S1 and S0 select signals, respectively, which are given as inputs to the multiplexer. The third and fourth waveforms indicate the value of the two operands X and Y, respectively, given as input to the ALU. The last two waveforms indicate the value of the output of the ALU and C_{out} of the half adder, respectively.

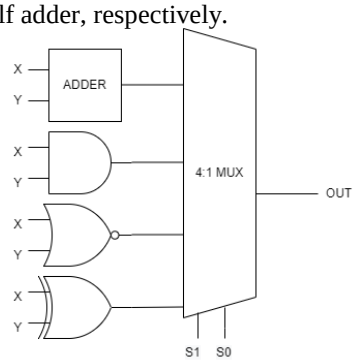


Fig. 4. Block Diagram of 1-bit ALU

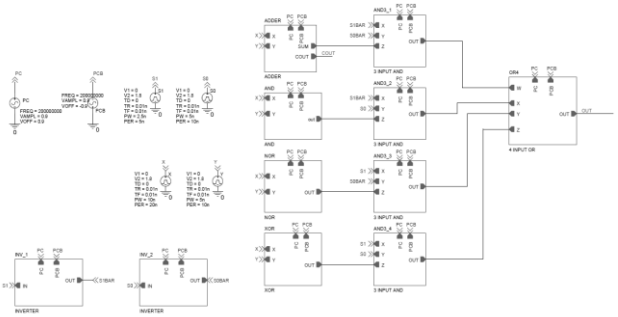


Fig. 5. WSDAL 1-bit ALU

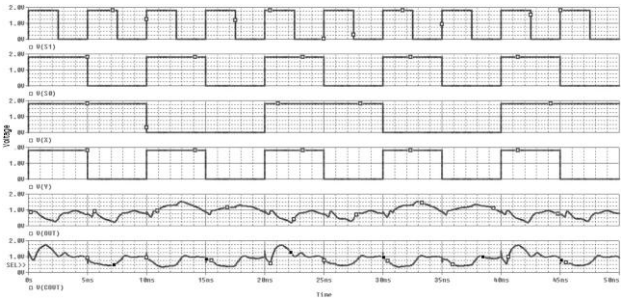


Fig. 6. Simulation Results of WSDAL 1-bit ALU

IV. RESULTS

The circuits are simulated in TSMC 180nm technology by using OrCAD Capture and PSpice. The W/L ratio is fixed for all transistors. The average power dissipated by the WSDAL circuit is calculated from Pspice simulations and compared to conventional CMOS designs for the relative improvement. The power dissipation of the circuits is analysed for power supply varying from 1.4V to 2.2V. The simulated results of WSDAL and CMOS ALU are shown in Table I. The relative comparison in Fig. 7, shows that the average power dissipation has been reduced by using WSDAL based implementation.

Table I. Power Dissipation of 1-bit ALU

Power Supply (V)	Power Dissipation (uW)	
	CMOS	WSDAL
1.4	1960.00	665.46
1.6	2574.88	905.17
1.8	3279.60	1210.57
2	4065.60	1559.76
2.2	4926.46	2008.02

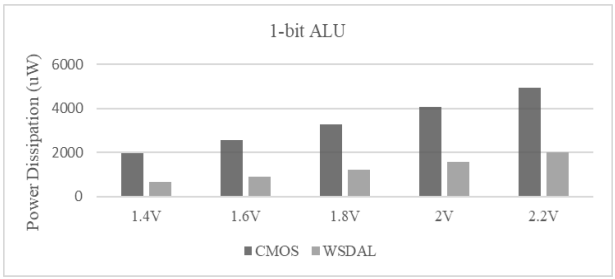


Fig. 7. Comparison of Power Dissipation of 1-bit ALU with varying Power Supply

V. CONCLUSION

This paper presents a comparative investigation of CMOS and WSDAL designs. The simulated results indicate that WSDAL based 1-bit ALU consumes less power than the conventional CMOS design at 200MHz. This work can be extended to design more complex multi-bit ALUs with added functionalities including multipliers and more logical functions.

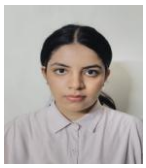
REFERENCES

1. D. Kumar and M. Kumar, “Comparative analysis of adiabatic logic challenges for low power CMOS circuit designs,” Microprocessors and Microsystems , vol. 60, p. 107–121, 2018. [CrossRef]
2. D. Kumar and M. Kumar, “VLSI implementation of wave shaping diode based adiabatic logic (WSDAL),” International Journal of Electronics, vol. 108, no. 4, p. 589–606, 2021. [CrossRef]
3. C. P. Anantha, S. Sheng and R. W. Brodersen, “Low-power CMOS digital design,” IEICE Transactions on Electronics, vol. 75, no. 4, pp. 371-382, 1992.
4. H. J. Veendrick, “Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits,” IEEE Journal of Solid-State Circuits, vol. 19, no. 4, pp. 468-473, 1984. [CrossRef]
5. S. Garg and V. Niranjan, “A new Cascadable Adiabatic Logic Technique,” Electrical and Electronics Engineering: An International Journal, vol. 5, no. 1, pp. 21-36, 2016. [CrossRef]
6. J. M. Rabaey and M. Pedram, eds. Low power design methodologies, Vol 336 Springer Science & Business Media, 2012.
7. G. Chaudhary, S. Garg and V. Niranjan, “Adiabatic Technique For Fat Tree Decoder To Be Used In Flash ADCs,” in National Systems Conference (NSC), 14-16 December 2015. [CrossRef]
8. M. T. Cutitaru, “IDPAL – A Partially-Adiabatic Energy-Efficient Logic Family: Theory and Applications to Secure Computing,” Ph.D. dissertation, Electrical/Computer Engineering, Old Dominion University, 2014. [CrossRef]
9. Y. Moon and D.-K. Jeong, “Efficient charge recovery logic,” in Digest of Technical Papers., Symposium on VLSI Circuits IEEE, 1995.
10. A. Vetuli, S. Pascoli and L. M. Reyneri, “Positive feedback in adiabatic logic,” Electronics Letters, vol. 32, no. 20, pp. 1867-1869, 1996. [CrossRef]

11. V. G. Oklobdzija, D. Maksimovic and F. Lin, “Pass-transistor adiabatic logic using single power-clock supply,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, no. 10, pp. 842-846, 1997. [CrossRef]
12. P. Sasipriya and V. K. Bhaaskaran, “Design of Low Power VLSI Circuits Using Two-Phase Adiabatic Dynamic Logic (2PADL),” Journal of Circuits, Systems and Computers, vol. 27, no. 4, 2018. [CrossRef]
13. D. Levacq, V. Dessard and D. Flandre, “Low leakage SOI CMOS static memory cell with ultra-low power diode,” IEEE Journal of Solid-State Circuits, vol. 42, no. 3, pp. 689-702, 2007. [CrossRef]

AUTHORS PROFILE

Ishita Khindria, received B.Tech. in Electronics and Communication Engineering from Indira Gandhi Delhi Technical University for Women, Delhi, India, in 2022. Areas of Interest are Low Power Design, Digital Systems Design, Microprocessors, and Microcontrollers.



Kashika Hingorani, received B.Tech. in Electronics and Communication Engineering from Indira Gandhi Delhi Technical University for Women, Delhi, India, in 2022. Areas of Interest are VLSI design, Digital Systems Design, and CMOS Circuits.

Prof. Vandana Niranjan, working as Professor in the Department of Electronics and Communication Engineering at Indira Gandhi Delhi Technical University Delhi, India. She graduated in the year 2000 and received her B.E. degree in Electronics and Communication Engineering from Government Engineering College (now University Institute of Technology of Rajiv Gandhi Proudyogiki Vishwavidyalaya) Bhopal. In the year 2002, she received her M.Tech degree from the Department of Electronics and Communication Engineering at Indian Institute of Technology (I.I.T) Roorkee with VLSI Design as specialization. In the year 2015, she was awarded her Ph.D. degree in the area of Low Voltage VLSI Design from University School of Engineering & Technology, GGSIP University Delhi. She has teaching and research experience of approximately 20 years at Indira Gandhi Delhi Technical University Delhi. Her areas of interest include MOSFET body bias techniques and Low-voltage Low-Power Analog CMOS circuit design. She has several publications to her credit in various international journals and conferences and book chapters.