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Low-Power 6T SRAM Cell using 22nm CMOS Technology

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Abstract: ***Static Random-Access Memory (SRAM) occupies approximately 90% of total area on a chip due to high number of transistors used for a single SRAM cell. Therefore, SRAM cell becomes a power-hungry block on a chip and it becomes more prominent at lower technologies from both dynamic and static perspective. Static power consumption is due to leakage current associated with the transistors that are off and dynamic power consumption is due to charging and discharging of the circuit capacitance. As gate length or channel length decreases gate oxide thickness also scales down. Scaling down of conventional transistor results in huge tunneling of electron from gate into channel leading to higher leakage power consumption. So, transistor with metal gate, high-k dielectric and strained-Si is used which shows better result in terms of low-power consumption, better performance with acceptable delay. Among various topologies of SRAM cell 6T is considered as a suitable choice for low power applications.***

Keywords**: *SRAM, Metal Gate/ High-k/ Strained-Si, Metal Gate/ High-k, Power Consumption***

I. INTRODUCTION

The conventional CMOS transistor tends to restrict the future scaling down of transistor due to several serious challenges such as mobility degradation, drain induced barrier lowering, low drain current, increased gate leakage current, subthreshold current, cost and difficulty in manufacturing. To achieve utmost scaling with better device performance transistors with metal gate, high-k and strained-Si is used. High-k means high dielectric constant, a measure of how much charge a material can hold. Higher-k material (e.g., HfO_2, ZrO_2, etc.) is physically thicker without being electrically thicker means 1nm SiO_2 based transistor and 4nm HfO_2 based transistor gives the same electrostatic but 4nm would decrease the tunneling of electron i.e., gate leakage current as gate now becomes physically thicker but it degrades the charge carrier mobility due to remote coulomb scattering and variations in material parameter. To improve charge carrier mobility strained-Si is used which means while manufacturing transistor silicon atoms are stretched beyond their normal interatomic distance which causes less resistance in the silicon and thus boosts up the device performance [1].

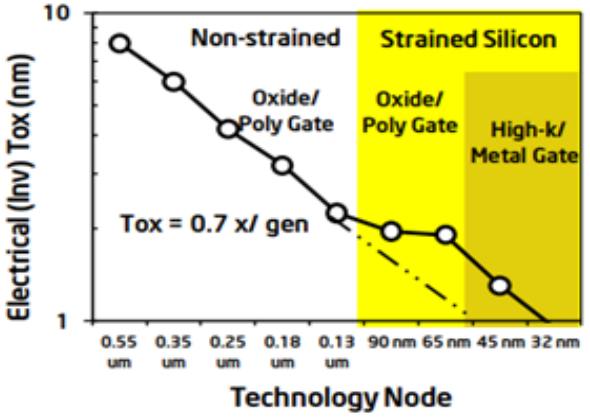

Fig. 1*:* CMOS transistor gate dielectric thickness scaling trend [2]

II. 6T SRAM CELL: OVERVIEW

A. Overview

6T SRAM cell consists of four transistors (P1, N1, P2, N2) joined back-to-back to form two cross-coupled inverters. Back-to-back feedback is used to maintain cell state. SRAM cell has two stable state 0 and 1.

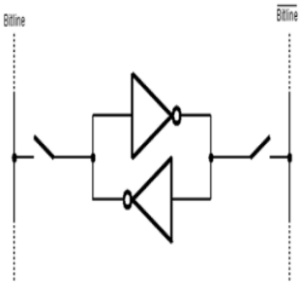

Fig. 2: Cross-coupled inverters

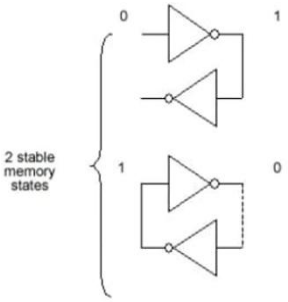

Fig. 3: Stable state of SRAM cell

Two additional access NMOS transistors (A1 and A2) connected to complimentary bit lines are used to control the access to a cell during read and write operations. Fig. (4) represents proposed 6T SRAM cell. Also, there are two storing nodes (Q and QB) and these storing nodes are read by the pass or access transistors. The gate of access transistors is connected to word line (WL) to have the data written to the memory cell from the bit lines.

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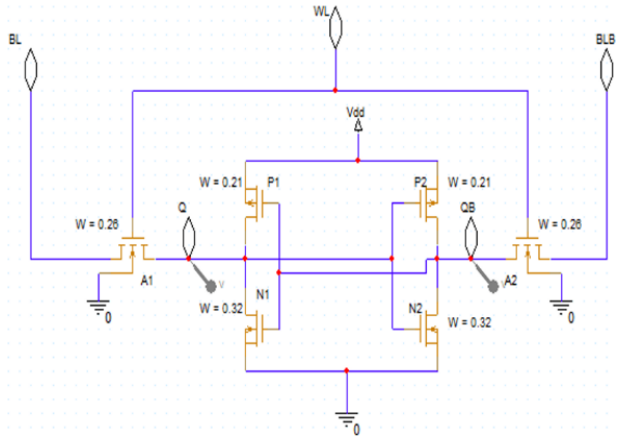

Fig. 4: Proposed Design

The Static Random-Access Memory cell performs three operations, hold (standby), read and write.

1.Standby: when circuit is idle

2.Reading: when data has been requested

3.Writing: when updating the contents

The access transistors are activated (during read and write operation) or deactivated (standby or hold mode) using the word line.

B.Steps involved in Read Operation

i) Pre-charge both bit lines to Vdd

ii) Turn ON word line (WL)

iii)Values at node Q and QB are transferred to complementary bit lines BL and BLB respectively

iv) One of the two-bit lines is pulled down by the cell

v) Voltage drops in the BL or BLB is sensed and amplified by the sense amplifier

vi) Sense amplifier determines value at node Q

(Decreasing BLB means logic '1' is stored in the cell and decreasing BL means logic '0' is stored in the cell)

C. Steps involved in Write Operation

i) Required data to be written is given to BL and its opposite data is given to bit line bar (BLB).

ii) Turn ON word line

iii) Bit lines overpower the cell with a new value

III. DATA STABILITY

Static Noise Margin (SNM) is defined as the minimum noise voltage at cell storage nodes (Q and QB) necessary to flip the state of the cell. Butterfly curve is used for determining SNM, read static margin and write static noise margin. Maximum square that can fit within the smaller wing of butterfly curve represents SNM of the cell. Butterfly curve is also used for determining static data stability during standby, read and write mode. There are two stable points during standby and read mode as shown in Fig. (5 &6) and one stable point during write mode corresponding to logic '0' and logic '1' as shown in Fig. (7 & 8) respectively. Intersection in the middle in read and hold SNM is not stable and two stable point correspond to two possible values stored by the cell, either zero or one [6].

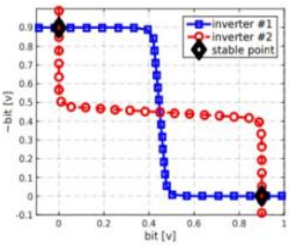

Fig. 5: Hold mode

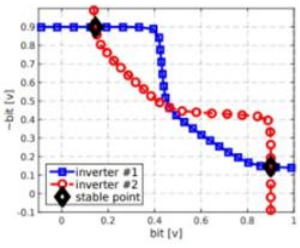

Fig. 6: Read mode

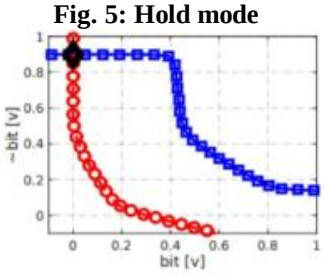

Fig. 7: Write logic '0'

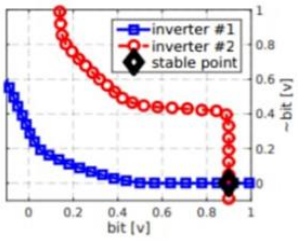

Fig. 8: Write logic '1'

A. Schematic for Determining SNM of SRAM cell [3]

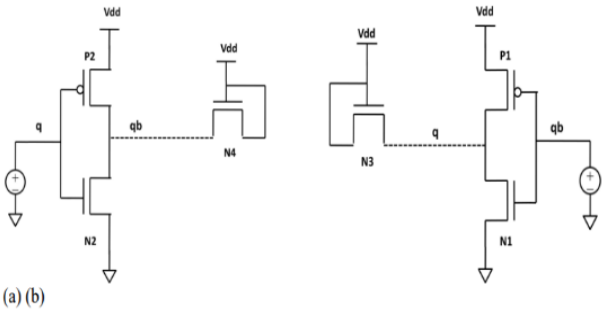

Fig. 9: Hold Mode

Dashed line means absence of connection between the circuits

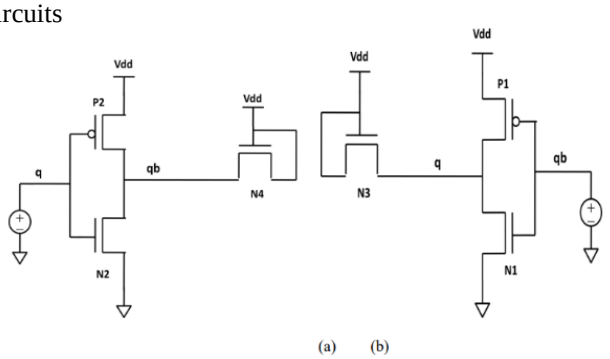

Fig. 10: Read Mode

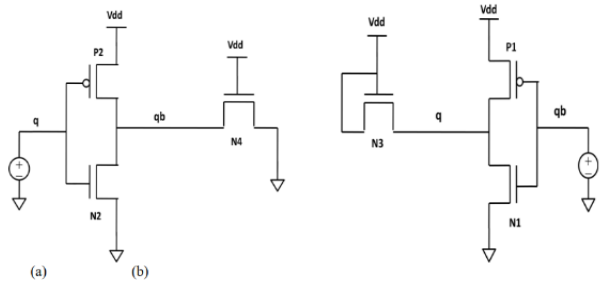

Fig. 11: Write Mode (logic '0')

B. Design Criteria

SRAM cell should be robust means W/L ratio should be such that when writing something the contents should get modified when input signal is applied and during read operation, we should be able to only read contents and not modify the contents.

*Read Operation

Inverter: Strong (means more W/L ratio)

Access Tx: Weak (means less W/L ratio)

*Write Operation

Inverter: Weak

Access Tx: Strong

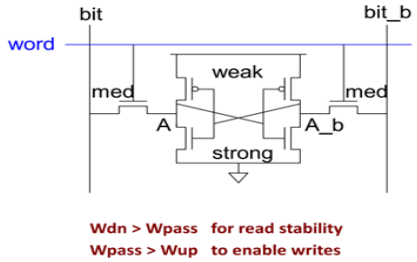

Fig. 12: Design Criteria

IV. PERFORMANCE PARAMETERS

Cell Ratio (CR): Cell ratio is defined as the ratio of pull-down transistor to the pass gate transistor. It is usually kept between 1 to 2.5 for better read operation.

Pull-up Ratio (PR): Pull-up ratio is defined as the ratio of pull-up transistor to the pass gate transistor. It is usually kept lower than 3 for better write operation.

Data Retention Ratio (DRV): It is the minimum VDD required for retaining the cell data in standby mode. It is slightly more than threshold voltage of MOS transistors.

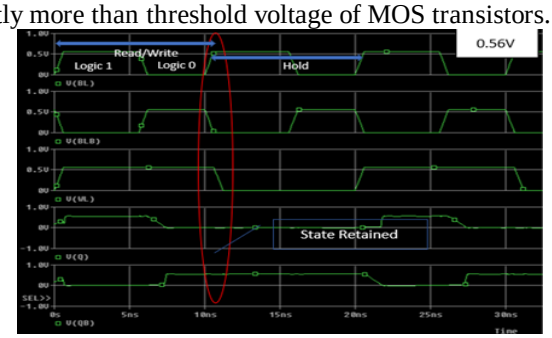

Fig. 13: State retention in hold mode at 0.56V

Read Access Time: It is defined as the time duration from the point when WL is activated to which 50mV difference is built across the complementary bit lines BL and BLB. Higher read access time means continuous switching takes place between V_{DD} to ground during read mode.

Write Logic '0' Access Time: It is defined as the time duration from the point when WL is activated to which the storage node, 'Q' (start with high level) reaches 10% of V_{DD} value for writing logic '0'.

Write Logic '1' Access Time: It is defined as the time duration from the point when WL is activated to which the storage node, 'Q' (start with low level) reaches 90% of V_{DD} value for writing logic '1'.

Power Consumption: Power Consumption can be reduced by reducing supply voltage, threshold voltage or capacitance. Reducing power consumption by lowering supply voltage is the most popular method as voltage has a quadratic relation to power. Reduction in supply voltage by a factor of two yields a factor of four decrease in power consumption but it increases the circuit delay. Reduction in threshold voltage increases the leakage current and reduction in capacitance has an adverse effect on cell performance. To improve cell performance, one needs to increase cell area which is bad choice in case of SRAM cell design.

V. SRAM CELL: SUCCESS VS FAILURE

Considering the design criteria of SRAM cell, its parametric failures such as read failure, write failure, and hold failure should also be taken into account.

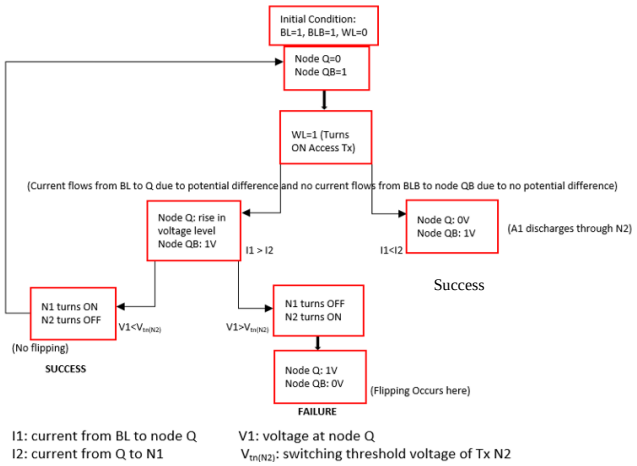

Fig. 14: Read mode [4]

Hold Failure:

Hold failure occurs when cell flip its state in hold mode. In scaled technology due to high subthreshold and gate leakage current at lower supply voltage there is high leakage of pull-down transistor which makes node storing logic '1' fall below supply voltage and if it falls below trip point of another inverter the cell tends to flips its state in hold mode. Reducing leakage current in standby mode using high threshold voltage pull-down transistors can reduce hold failure rate but this comes at the price of read delay [7].

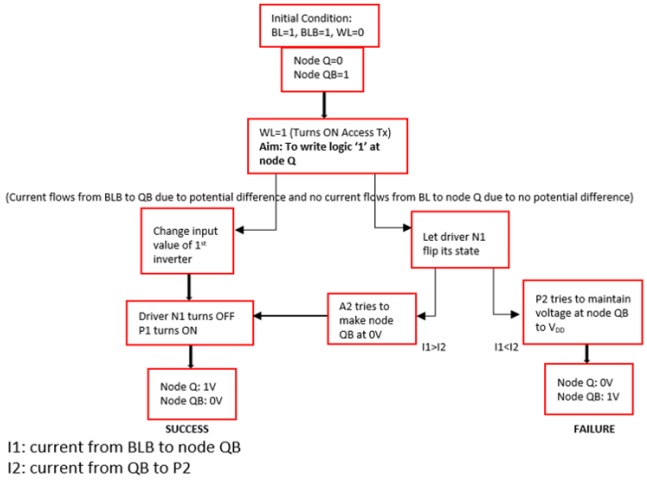

Fig. 15: Write Mode [5]

VI. RESULTS AND DISCUSSION

This section discusses simulation result and performance analysis of conventional 6T SRAM cell in 22nm CMOS technologies using two different PTM model (model for metal gate/ high-k/ strained-Si (Design 1) and metal gate/ high-k (Design 2)) with the help of Pspice tool. Parameters used for SRAM cell designing are shown in Table-I. Fig. (16) and Fig. (17) shows that DRV depends on pull-up ratio and cell ratio and it increases with increase in pull-up or cell ratio. Fig. (18) shows that static power consumption increases with increase in supply voltage and is less for design 1 for all supply voltage. Fig.(19) shows that dynamic power consumption increases with increase in supply voltage and remains same for both the designs. Read access time and write access time decreases with increase in supply voltage as shown in Fig. (22, 23 & 24) respectively. Table-II depicts the comparison of both the designs at 0.6V power supply. Design1 shows better performance in terms of both read and write operation as its read and write static noise margin is higher as compared to design 2 Fig. (20 & 21). For both the designs cell retained its state in standby mode for voltage range from 0.56V to 0.64V. Although having state retention at 0.56V and 0.57V, write and read instability occurs as shown in Fig. (25) and Fig. (26). Also, at 0.64V there is read instability in design 2 due to increase in number of intersection points between two stable points as shown in Fig. (27). Write instability occurs when there is two intersection point in write SNM corresponding to one logic state.

Table-I: Parameters Used

Parameters	Value
Level	3
L	22nm
$(W/L)_{PU}$	0.21/0.022
$(W/L)_{PD}$	0.32/0.022
$(W/L)_{PG}$	0.26/0.022
CR	1.2
PR	0.86
DRV	0.56V
Vtp	-0.4606V
Vtn	0.50308V
V_{DD}	0.6V
Temperature	27 °C

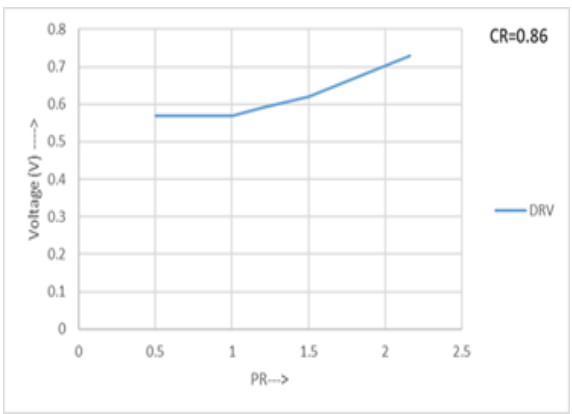

Fig. 16: DRV variation with increase in Pull-up ratio

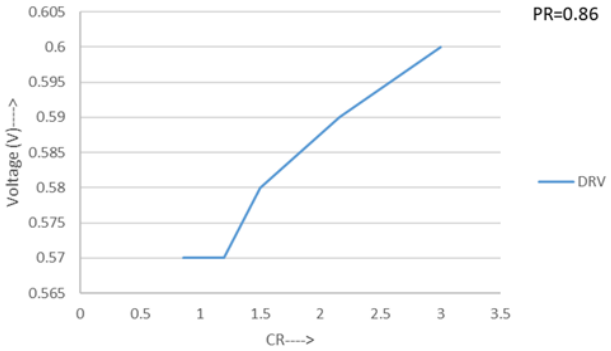

Fig. 17: DRV Variation with increase in Cell ratio

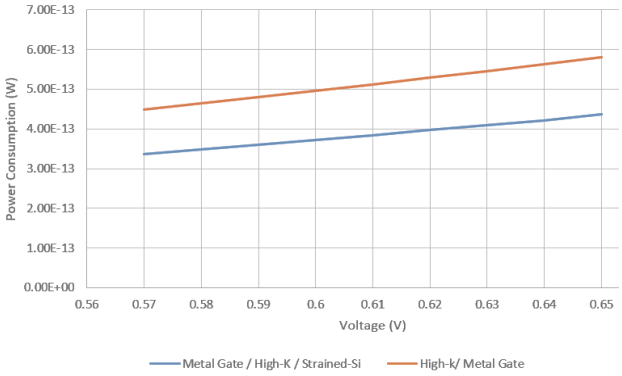

Fig. 18: Static Power Consumption

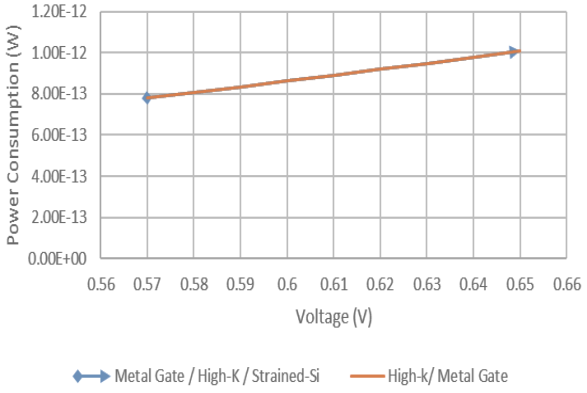

Fig. 19: Dynamic Power Consumption

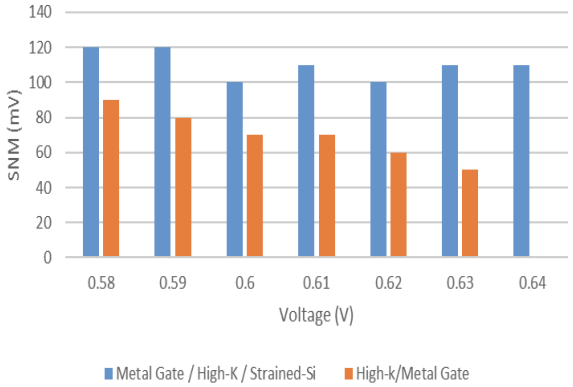

Fig. 20: Read static noise margin

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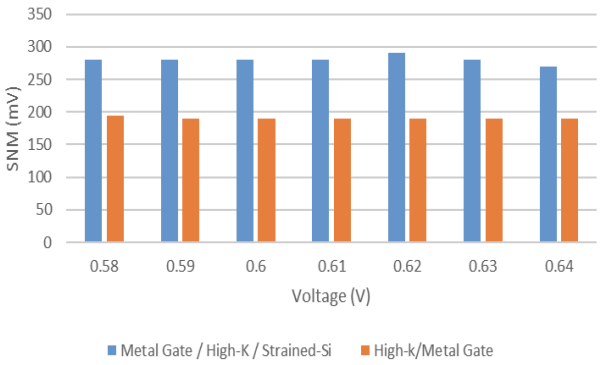

Fig. 21: Write static noise margin

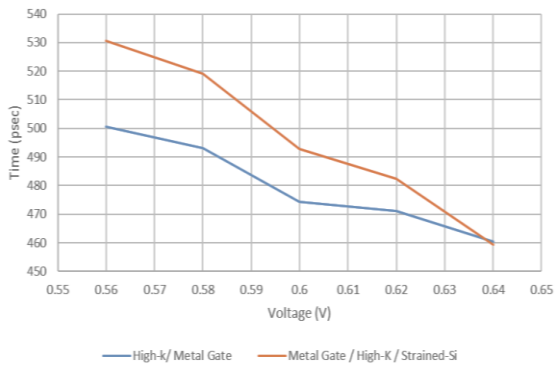

Fig. 22: Read access time

Table-II: Comparison: Design 1 and Design 2 at 0.6V

Design	Voltage (V)	RSNM (mV)	WSNM (mV)	Static Power Consumption (pW)	Dynamic Power Consumption (pW)	Read Access Time (pSec)	Write '0' Access Time (pSec)	Write '1' Access Time (pSec)
Design 1	0.6	100	280	0.372	0.862	492.857	740.406	784.262
Design2	0.6	70	190	0.496	0.862	474.384	761.875	741.757

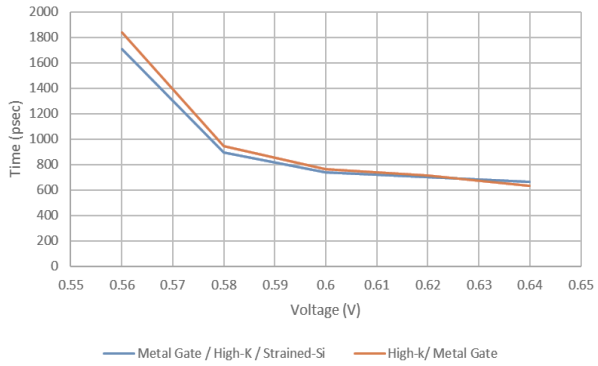

Fig. 23: Write logic '0' access time

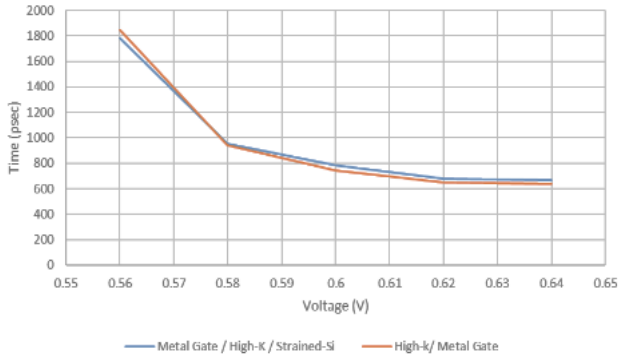

Fig. 24: Write logic '1' access time

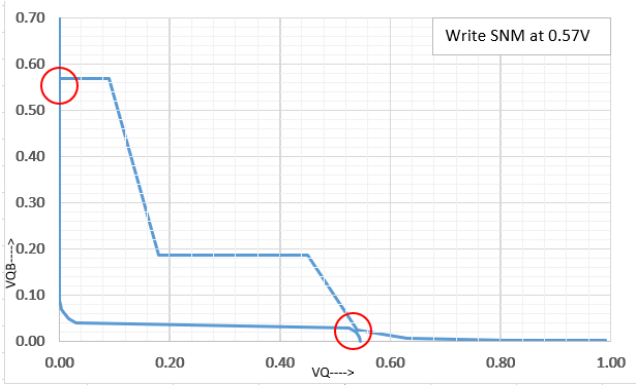

Fig. 25: Write instability at 0.57V

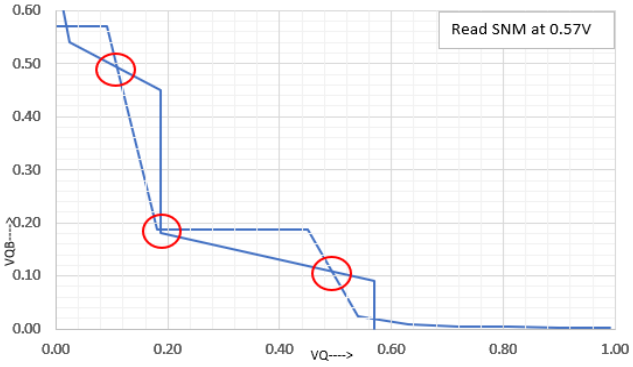

Fig. 26: Read instability at 0.57V

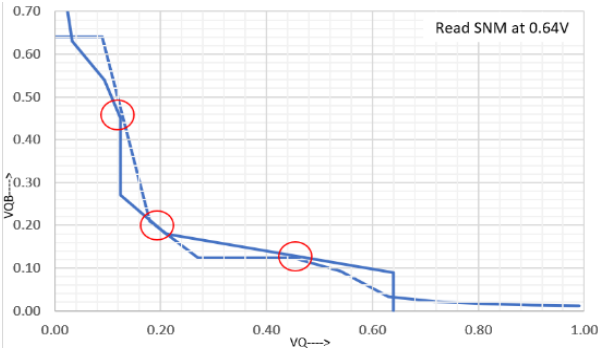

Fig. 27: Read instability at 0.64V

VII. CONCLUSION

Proposed designs operate better in terms low-power consumption, better performance and acceptable delay at 0.6V. Design 1 shows better result. On comparing results obtained for design 1 & design 2 with that in [3] for 22nm CMOS technology, 98.4% reduction in static power consumption, 99.9% reduction in dynamic power consumption is obtained and 99.86% reduction in total power consumption. Also, read static noise margin and write static noise margin has improved when metal gate/ high-k/ Strained-Si (i.e, Design 1) transistor model is used.

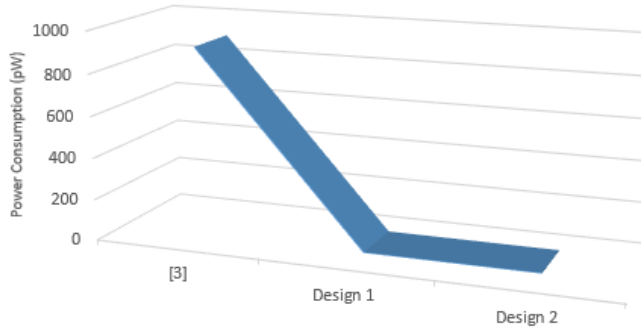

Fig. 28: Dynamic power consumption

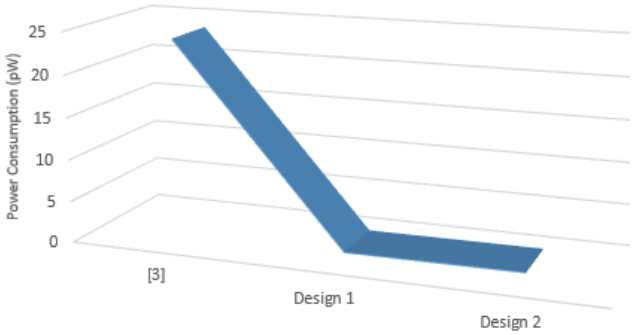

Fig. 29: Static power consumption

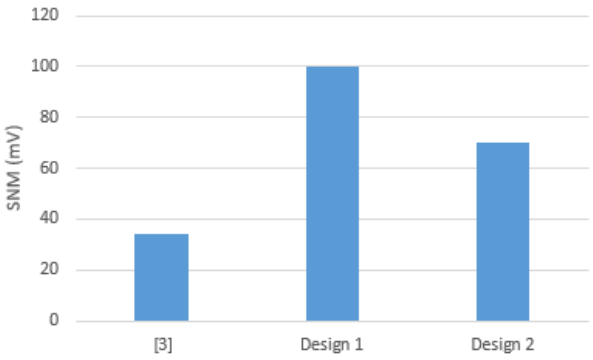

Fig. 30: Read static noise margin

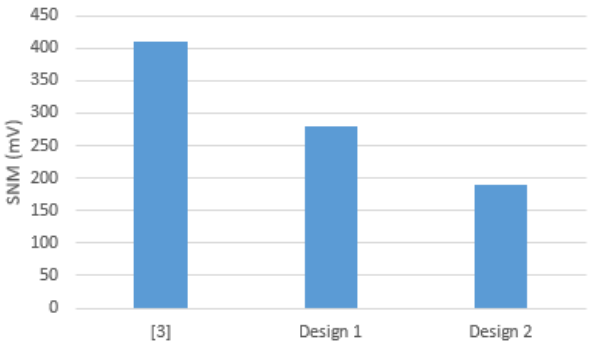

Fig. 31: Write static noise margin

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REFERENCES

1. Sharma, Rajneesh. and Rana, Ashwani, K. (2015). Strained-Si: Opportunities and Challenges in Nanoscale MOSFET. Proceedings of the 2nd International Conference on Recent Trends in Information Systems (ReTIS); July 9-July11, 2015; IEEE, Kolkata, India, p. 475-480. [CrossRef]
2. Jan, C. and Agostinelli, M. (2010). RF CMOS technology scaling in High-k/Metal gate era for RF SoC (System-on-chip) applications. Proceedings of the International Electron Devices Meeting; December 6-December 8, 2010; IEEE, San Francisco, CA, USA, p. 27.2.1–27.2.4. [CrossRef]
3. Saun, Shikha. and Kumar, Hemant. (2019). Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization. Proceedings of the IOP Conference Series: Materials Science and Engineering; April 12-April 13, 2019; IOP Publishing Ltd, Hotel Aloft, Coimbatore, Tamil Nadu, India, p. 1-9. [CrossRef]
4. Mande, Sudhakar. (2015). Design of 6T CMOS SRAM. Kurla, Mumbai, India. Available from: www.youtube.com/UC-piW0uDmr0Je8rbxMv4qg. Accessed date: September 19, 2015.
5. Acolyte. (2020). SRAM Memory Unit. United States. Available from: https://youtube/IYFPo6OM3hE. Accessed date: June 6, 2020.
6. Royer, Pablo. (2015). Design and Simulation of Deep Nanometer SRAM Cells under Energy, Mismatch, and Radiation Constraints, [Ph.D. thesis]. University Polytechnic Madrid, 177p.
7. Islam, A. and Hasan, M. (2011). Single-Ended 6T SRAM Cell to Improve Dynamic Power Dissipation by Decreasing Activity Factor. The Mediterranean

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