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Design of Smart Alu with Error Detection and Correction at Input Side

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Abstract: ***We are moving towards the era of scaling down of transistor size, short channel effects (SCEs) and errors are becoming major concern. NSFET is emerging transistors, which gives better SCEs performance compared to conventional MOSFET and FinFET transistors. In this paper, (7, 4) Hamming code was implemented at input side of ALU to prevent error which occur when the transistors size decreases (scale down). The efficiency of any system depends on the performance of internal components. If internal components satisfy the criteria of area, power and delay, the system will always be a efficient system, therefore in this paper the smart ALU was designed by making the internal components to satisfy criteria of area, power and delay. All internal components of ALU including (7, 4) Hamming code was designed by using MICROWIND 3.9 and DSCH 3.9 software and each component design was started from schematic diagram and moved up to automatic physical design by using Verilog code and including post layout simulation with spice netlist which contains parasitic parameters and finally area, power consumption, propagation delay including global delay analysis with RC information and operating frequency of each internal components of ALU was measured and compared with existing one and also Number of error detected and corrected was measured. Two kind of technology was used depending on their advantages (3nm technology for arithmetic design and 7nm technology for remain component design).***

Keywords: ***NSFET, Fin FET, SCEs, Error, (7, 4) Hamming code, MICROWIND 3.9, DSCH 3.9, schematic diagram, physical design, Verilog code.***

I. INTRODUCTION

1.1 Background

The key to any IC is the transistor. Walter Brattain invented the first transistor in 1947 with the help of John Bardeen and named it the point-contact transistor. The device was made of two gold contacts on a germanium crystal. In 1951, William Shockley developed a transistor, which revolutionized electronics. This is a big change in transistors - the first junction transistor is made of P- and N-type germanium semiconductor layers.

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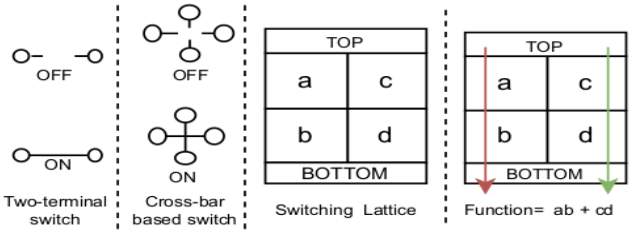


The second big change in transistor evolution came with the development of the field-effect transistor in the 1960s. Modern transistors are field-effect transistors made of metal-oxide semiconductor materials. The fundamental block of Portable applications such as mobile phones, laptops, iPhones is IC and there is a huge demand for them with a low amount of power consumption, a minimum area and quick operation. Therefore, circuits that provide low power consumption minimum area and high switching speeds are likely to be the best candidates for design of microprocessors and other subsystems [1]. To meet these specifications, we should work our way down to the circuit level. To get the better performance of device parameters such as size, delay, speed and power continuous scaling of device is required. However, continuing to scale MOSFETs below 45nm node technology results in short channel effects (SCE's), which can have a negative impact on device performance. To overcome the disadvantage of MOSFETs, FinFET was developed.

1.2 ALU

CPU can be divided in to a control section and data section. Control section issues control signal to data path. This thesis focus on only Data Path, Data section is also called data path and it contains Registers and ALU. A register is a small amount of storage available as part of a CPU. Arithmetic and Logic Unit (ALU) is a combinational circuit which perform arithmetic as well as logic operations. It is mathematical brain and fundamental building block of central processing unit of a computer. Figure 1.1 show that from where does this operands come.

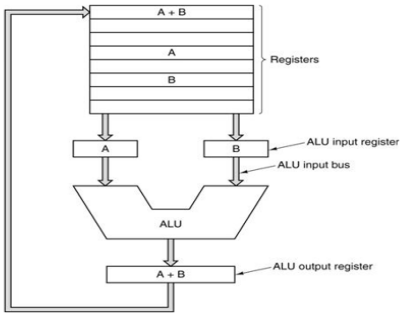


Figure 1.0 1 Data Path

1.3 FinFET Technology

FINFET known as Fin Field Effect Transistors non-planar or 3D transistor used to design modern processor. The main characteristics of FINFET is that it has a conducting channel wrapped by a thin silicon "fin" and hence the name FINFET. The thickness of the fin determines the effective channel length of the device. This fin allows multiple gates to operate on single transistor. The multiple gates of FINFET extend Moore's Law which allows the semiconductor manufacturers to create microprocessor subsystem and memory modules that provides faster performances, less energy consumption and reduction in space complexity. It was developed at the university of Berkley California by Chenning Hu and his colleagues. FINFET's are multiple gate devices. These multiple gates provide better control over the channel and hence reduce the short channel effects [1]. In FinFET the NMOS in CMOS technology is replaced with N-Finfet and PMOS with P-Finfet, both gates of Finfet are together. FinFETs are popular devices that are used in foundries till the latest 5nm node. However, studies forecast that this will come to an end starting from the sub-5nm processes [2]

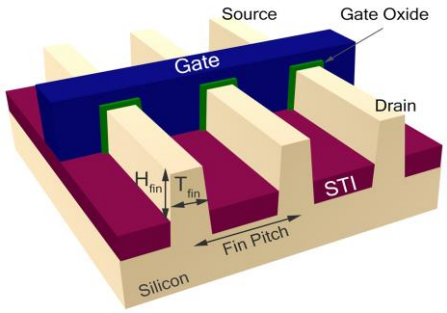


Figure 1.0 2 3D Structure of FinFET [3]

1.4 NANO-SHEET Technology

The type of the transistor that the researcher used is Nano sheet FET, which is very novel. In 2019, Samsung Electronics Company announced to modernize the process of a new node technology with 3nm Nano-sheet [4]. This technology will represent a huge advancement in the world computing, and overcome all current physical limitation and electrical constraints. In recent technology, the Nano-sheet Transistor is earning extremely high attention because it over comes on the physical limitation and fabrication challenges of the FinFET technology [5]. NSFET structure has a gate all around configuration that similar to the NWFET but unlike the structure of FinFET, its channel width is not limited, it is based on GAAFET.

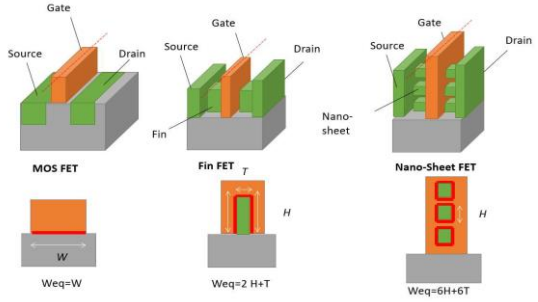


Figure 1.0 3 MOSFET, FinFET & Nano-Sheet FET, with Corresponding Equivalent Channel Width [6]

It can be seen from Figure 2.4 that inside a discounted silicon surface, system engineers were capable of fabricate a great deal greater green gadgets than the authentic MOSFET, in particular in phrases of equal channel width (W) this is almost proportional to the switching current. Stacking nano sheets permit an equal channel width greater than three instances greater area-green than the MOSFET, in its three stacked nano-sheet configuration.

1.5 Error Detection and Correction code

Errors occur in VLSI circuit due to radiation, temperature changes etc. Reliability is a major concern in advanced electronic circuits. To improve system reliability, we need an automatic error detection and correction circuit. Errors caused by radiation become more common as technology scales. To ensure that those errors do not affect the circuit functionality a number of mitigation techniques can be used. Among them, Error Correction Codes (ECC) are commonly used to protect memories and registers in electronic circuits and Hamming code is one of such forward error correcting code which has got many applications. Hamming code are the linear block code which are invented by Richard. W. Hamming. It is an error correction code that is used in the process of detecting single and 2-bit errors and corrects the single-bit error that may happen when binary data is propagated along the way from one unit into another. There are two main parts in hamming code and they are encoder and decoder.

a) Hamming Encoder

The main function of encoder is to encode data or to generate parity bit and the minimum number of parity bit is depend on the type of hamming code. For example the minimum number of parity bit of (7,4) hamming code is 3 which is generated from $2^P \geq P + M + 1$, where P is number of parity bit, M is number of message bit. The parity bits are placed at positions corresponding to power of 2 (1, 2, 4…) and hamming encoder generate parity bit as follows:- $P_1 = D_3 \oplus D_5 \oplus D_7$, $P_2 = D_3 \oplus D_6 \oplus D_7$ and $P_4 = D_5 \oplus D_6 \oplus D_7$ and here below the table which show the positions of each parity bit.

Table 1.0 1 Position of Parity Bits

Position	7	6	5	4	3	2	1
Code word	D_7	D_6	D_5	P_4	D_3	P_2	P_1

Combination of data and parity bit is what we call code word and it is used as an input for the encoder circuit which performs XOR operations on the given data word and the below table show code word of each data.

Table 1.0 2 Data Word and Code Word of (7, 4) Hamming Encoder

Data Word	Code Word
0000	0000000
0001	0001111
0010	0010011
0011	0011100
0100	0100101
0101	0101010

0110	0110110
0111	0111001
1000	1000110
1001	1001001
1010	1010101
1011	1011010
1100	1100011
1101	1101100
1110	1110000
1111	1111111

b) Hamming Decoder

The main function of hamming decoder is to decode the received data and it consists of checker bit generator, 3 to 8 decoder and XOR gates. In this circuit, the code word is applied as an input then the check bits are generated by the checker bit generator, these bits are given to the decoder that enables the XOR gate which is having the error. Depending on the correction algorithm either it will be detected or corrected.

1.6 Compact Model

Compact models for semiconductor devices are essential for all types of electronic designs. Analog, digital, or mixed signal circuits are always carefully implemented and tested by circuit simulators where compact models are used to represent, in a mathematical form, the electronic behavior of each device.

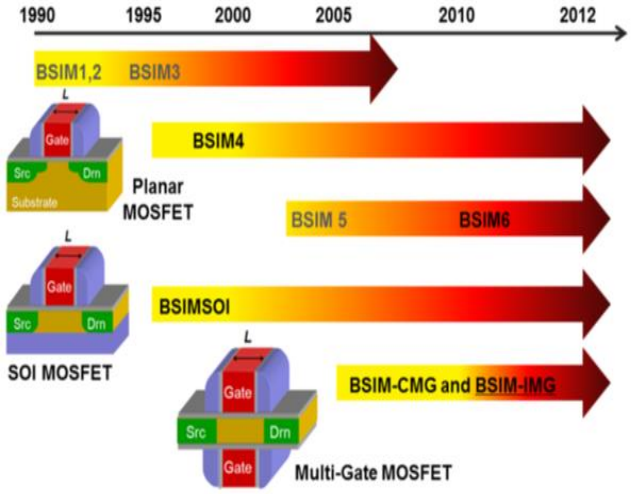


Figure 1. 0 4 BSIM Family of Compact Models

1.7 Short Channel Effects (SCEs)

MOSFET scaling could not continue forever at the same rate of Moore's law. Shrinking the gate length Lg degrades the transfer characteristics of a planar MOSFET; the subthreshold swing SS degrades and Vth decreases (the effect known as Vth roll-off), which implies that the device cannot be turned off easily by lowering the gate voltage, Vg. These problems are collectively known as short channel effects (SCEs).

1.8 MICEOWIND 3.9 and DSCH 3.9

The MICROWIND is truly integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination and it allows the student to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. New features & functions added to the 3.9 Version are introduction of Nanosheet Field Effect Transistor (NSFET) with 3nm technology, introduction of 5nm and 7nm FinFET Transistor technologies, multiple Verilog file compilation with layout position control.

The **DSCH** program is a logic editor and simulator. It is used to validate the architecture of the logic circuit before the microelectronics design is started and it can generate Verilog from schematics.

1.2 Organization of Paper

This paper starts with the introduction providing back-ground information of the topic with problem statement and objectives of study, next unit provides information regarding literature review and gap analysis, the 3rd chapter discusses about method and materials, 4th chapter provides information regarding result and discussion and last section talks about summary, conclusion and future works.

II. LITERATURE REVIEW

A lot of designs have been proposed to implement ALU with different techniques such as Pass transistors, Transmission gate, CMOS, FinFET based etc. in order to reduce number of transistor counts. The performance of ALU can be enhanced for features like power and area by optimizing standard cell blocks. According to [1] the MOSFET and FinFET based full adder cell for 28T and 16T at different nodes was characterized. The obtained results for the FinFET full adder spice models used here shows a promising solution for MOSFETs scaling issues. The power dissipation in 28T FinFET based adder at 14nm is reduced to 32nW from 62nW at 22nm adder, similarly delay get reduced from 25ps to 13.9ps when node size is reduced from 22nm to 14nm node. Likewise, the results for the power and delays values for sum and carry operation are for 16T FinFET based full adders. The speeds of the adder circuits are increased terms of the sum and carry delay operation. According to [2] the researcher confirmed the performance of 3nm Nano sheet FET (NSFET) from the perspective of VLSI which has inspired me. FinFET is best alternative to solve challenges that happens in planer MOSFET beyond 22nm technology, and FinFET very much effective to avoid short channel effect. There is some limitation of it i.e., beyond 5nm technology it can't be used [5]. Reviews and presents the performances of NSFET and make a comparison with other nano-structure transistors like FinFET and NWFET in [4]. By using the mentor graphics tool the proposed circuit of the 11 transistor half adder half sub tractor cell have been obtained by using the finfets [7]. The designs of low power ALU using finfets have been completed up to the half adder and half sub-tractor cells. In [6] the NSFET characteristics, the performance tradeoff, interconnect parasitic effects and the performances of basic cells such as logic gates, ring oscillators and memory cells was discussed and according to it the 3-nm node enables 20% speed improvement or 25% area saving as compared to the 5-nm FinFET-based node.

The 8-bit ALU was designed in [8] using MOSFET and Independent gate FinFET for 32nm technology and according to it the designed ALU performs a total of 24 operations of which one is arithmetic, 7 are logical and the remaining are shift and rotate operations. According to [9] the design of 4-bit ALU was implemented by categorizing it into different blocks and every block in ALU was individually optimized to achieve low power and area efficiency.

In [10], the design and analysis of Arithmetic and Logical Unit (ALU) circuit was designed using CMOS technology as well as speed performances. A complete architecture, design & implementation of 2-bit ALU slice was described in [11]. According to [12] Designing of ALU using FinFET 32nm technology was done to minimize the leakage power, leakage current and operating power of an ALU.

The design of the 4-bit ALU was proposed by using the sub blocks of full Adder, 4xl and 2xl multiplexers, and gates like exclusive or, and, or and inverter in [13] which has inspired the design of my own circuit. 8-bit ALU design using 11-T FA and GDI based multiplexer at 65nm technology was proposed in [14]. 1-bit ALU was designed by using MOSFET and FinFET using the sub blocks of full adder, full subtractor, AND gate, OR gate and 4:1 multiplexer in [15].The design of 8-bit ALU was implemented by categorizing it into different blocks in [16].The design of 8-bit ALU here is employs DG-FinFET's 45nm technology and the area of ALU is optimized by lessening the count of transistors in the implementation of individual operation.

2.1 Research Gap Analysis

[17] and [18] recommended that extending to high number of bit.

[18] Recommended to design ALU with some error detection and correction code to get high performance, low power and fault secure codes.

[21] More recommended to extend bit number and technology node.

[5] Said that below 5nm FinFET is not reliable ,channel mobility decreases and again leakage becomes a big issue ,power dissipation of device increases so they suggested a new technology (NSFET).

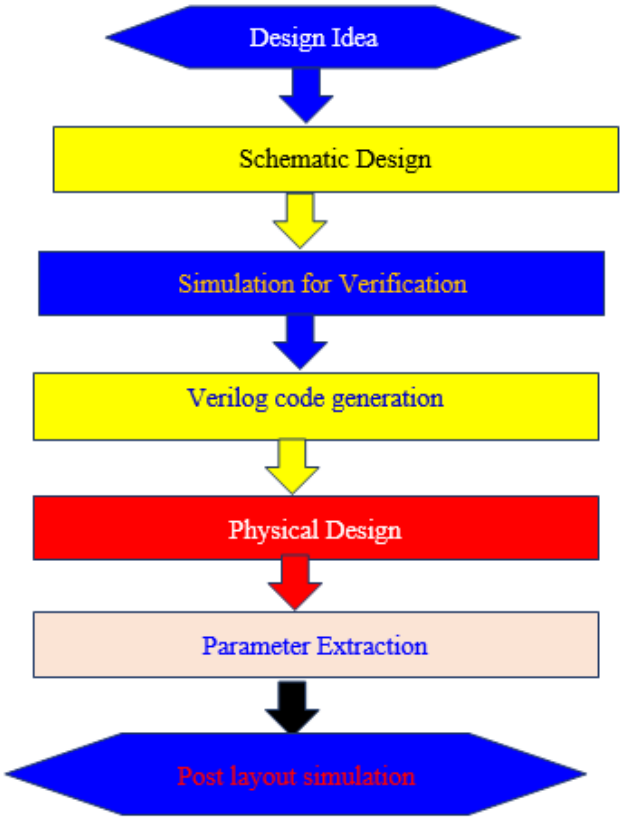
[1] Suggested that their proposed system can be further extended to the full adders, full sub-tractors, the carry look ahead adders, and the ripple carry adders.

III. MATERIALS AND METHODS

3.1 ALU Design Methodology

The researcher divided the proposed ALU module in to 4 basic sub-module like Arithmetic, Logic, multiplexer and Hamming code. Each module was designed separately by following the above flow chart and then recombined together to gate proposed ALU module.

3.2 Design Flow



Arithmetic Module Design Method

The proposed arithmetic module performs two operations such as addition and subtraction of two 8 bit operands. The researcher used the following procedure and techniques as general guideline to design Arithmetic module.

- Functions of 1 bit Full Adder was stated by using truth table.
- Schematic of 1 bit full adder circuit was drown in DSCH 3.9.
- 2x1 MUX was designed by using pass transistor logic.
- 1 bit full adder and 2x1 MUX was combined together to get 1 bit full adder/subtracter.
- Simulation of 1 bit full adder/subtracter was performed and Timing diagram was observed.
- Verilog code was generated from 1 bit full adder/subtracter
- Threshold voltage, ION vs IOFF, Ids vs Vds and Id vs Vg curve of both Fast and Slow NSFET were observed in MICROWIND by using BSIM4
- Layout of 1 bit full adder/subtracter was generated automatically by using generated Verilog code.
- Parameter extraction and Post layout simulation of 1 bit full adder/subtracter had done.
- 8 bit Ripple Carry Adder/Subtracter was designed by combining eight 1bit full Adder/Subtracter.
- Designed 8 bit Ripple Carry Adder/Subtracter was simulated in DSCH3.9 and Timing diagram was observed.

- Verilog code of 8 bit Ripple Carry Adder/Subtracter was generated.
- Layout was generated automatically.
- Parameter extraction and Post layout Simulation was carried by using MICROWIND3.9.
- Power consumption, Area, delay and speed of 8 bit Adder/Subtracter was measured.

Logic Module Design Method

The logic module performs three bitwise logic operations, such as AND, OR and NOT. The researcher used the following the procedures to design Logic Module of ALU.

- Semi-custom design style was used
- Schematic of 1 bit AND, OR, and NOT logic gate was drown by using PMOS and NMOS in DSCH.
- Schematic was converted in to layout automatically.
- Simulation of schematic as well as layout was carried out.
- Power dissipation, Area, delay and speed of each logic gate was calculated.
- 8 bit AND, OR, and NOT logic gate was designed.
- Schematic diagram was verified and timing diagram was observed.
- Layout diagram of 8 bit logic gate was developed automatically.
- Parameter extraction and Post layout simulation was performed.
- Power dissipation, Area, delay and speed of 8 bit logic gate was calculated.

Multiplexer Module Design Method

Researcher used eight 2x1 MUX and eight 4x1 MUX. The main purpose of MUX is to select one output among different inputs based on the selection line and 2x1 MUX for selection of either Addition or Sbtraction and 4x1 MUX for selection of one output among 4 inputs (Arithmetic, AND, OR and NOT). The followings are the steps followed by the researcher.

- 2x1 Mux was designed by using pass transistor logic in DSCH.
- 4x1 Mux was designed by using three 2x1 Mux
- Schematic of 4x1MUX was converted in to layout
- Parameter extraction and Post layout simulation was performed.
- Area, speed, power and delay of one 4x1 Mux was measured.
- Finally the Schematic of 8 bit ALU was drown by combining all 3 modules and simulation was performed.
- Total Area, Power consumption of 8 bit ALU without error detection and correction circuit was calculated

Error Detection and Correction Code Design Method

The researcher tried to incorporate error detection and correction code to ensure that the inputs of ALU are free from error. To do this the researcher followed the following steps:-

- Hamming encoder (HE) and Hamming decoder (HD) was designed at gate level by using DSCH3.9.
- 4bit register was designed by using D ff in DSCH.
- Designed HE and HD was implemented before and after 4bit register respectively.
- Error circuit was designed to verify designed Hamming code (HC).
- Parameter extraction and simulation of proposed HC was performed at schematic level as well as post layout level.
- Power consumption, Area, delay and speed of proposed HC was calculated.
- Interface of designed HC and 8 bit ALU was done.
- Power consumption, Area and number of detected and corrected error of proposed 8 bit ALU with error detection and correction at input side was calculated.

Block Diagram of the Proposed ALU Circuit

The block diagram of proposed ALU circuit composed of 7 major blocks. They are Hamming Encoder (HE), Register, Hamming decoder (HD), one 2x1 MUX, one 4x1 MUX, Arithmetic (+/-) and Logic block (AND, NOT, OR). A and B are the two operands, Cin is carry in, Cout is carry out, S0 is selection line for 2X1 MUX and S1,S2 are selection line of 4x1 MUX. The operation of ALU can be Addition, Subtraction, AND, NOT, OR depending on the value of S0, S1, S2.

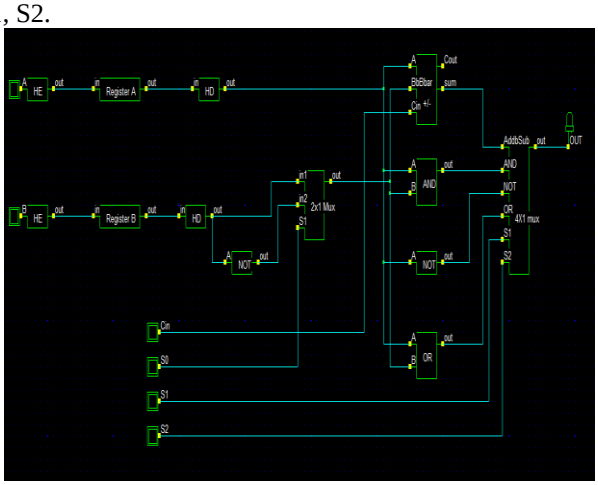


Figure 3.0 1 Blok Diagram of Proposed ALU (DCSH 3.9)

IV. RESULTS AND DISCUSSION

4.1 Introduction

In this chapter overall works done by the researcher and it's results was discussed. The first section discuses about simulation result of Arithmetic part, the second section discuses about the simulation result of MUX part, the 3rd section discuses about the simulation result of logic part, the 4th section discusses about the simulation result of (7, 4) hamming code, the 5th section discusses about the simulation result of overall 8 bit ALU with and without error detection and correction code at input side.

Before starting the design, the threshold voltage, ION vs IOFF, Ids vs Vds and Id vs Vg curve of both Fast and Slow NSFET were observed in MICROWIND by using BSIM4.

Figure 4.0 1 Id vs Vd Curve of p-type NSFET using BSIM4

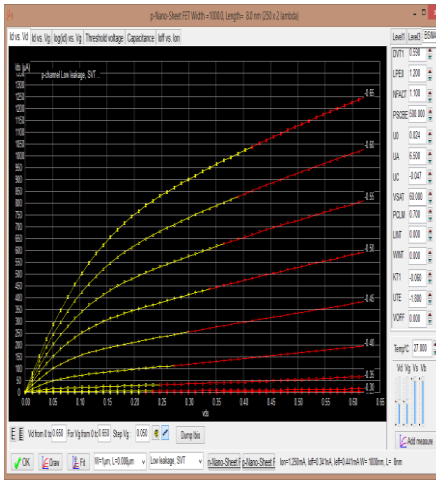


Figure 4.0 2 Threshold Voltage of P-NSFET

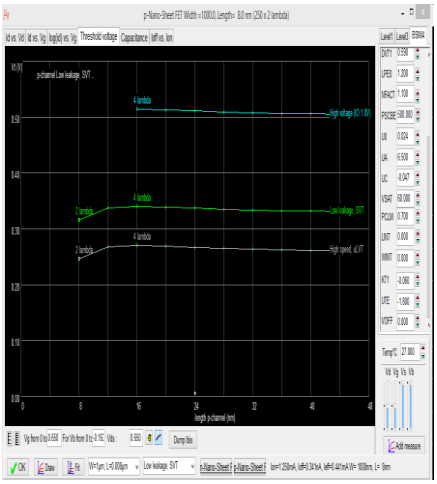


Figure 4.0 3 Id vs Vg Curve of P-NSFET

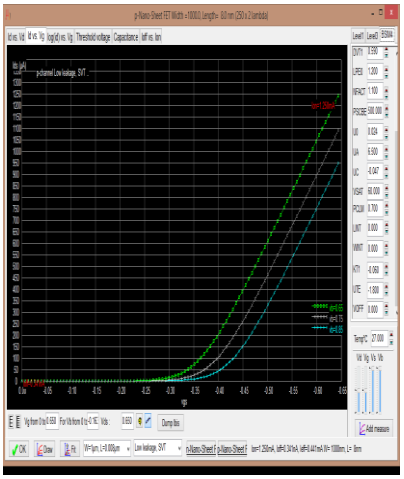


Figure 4.0 4 N type NSFET

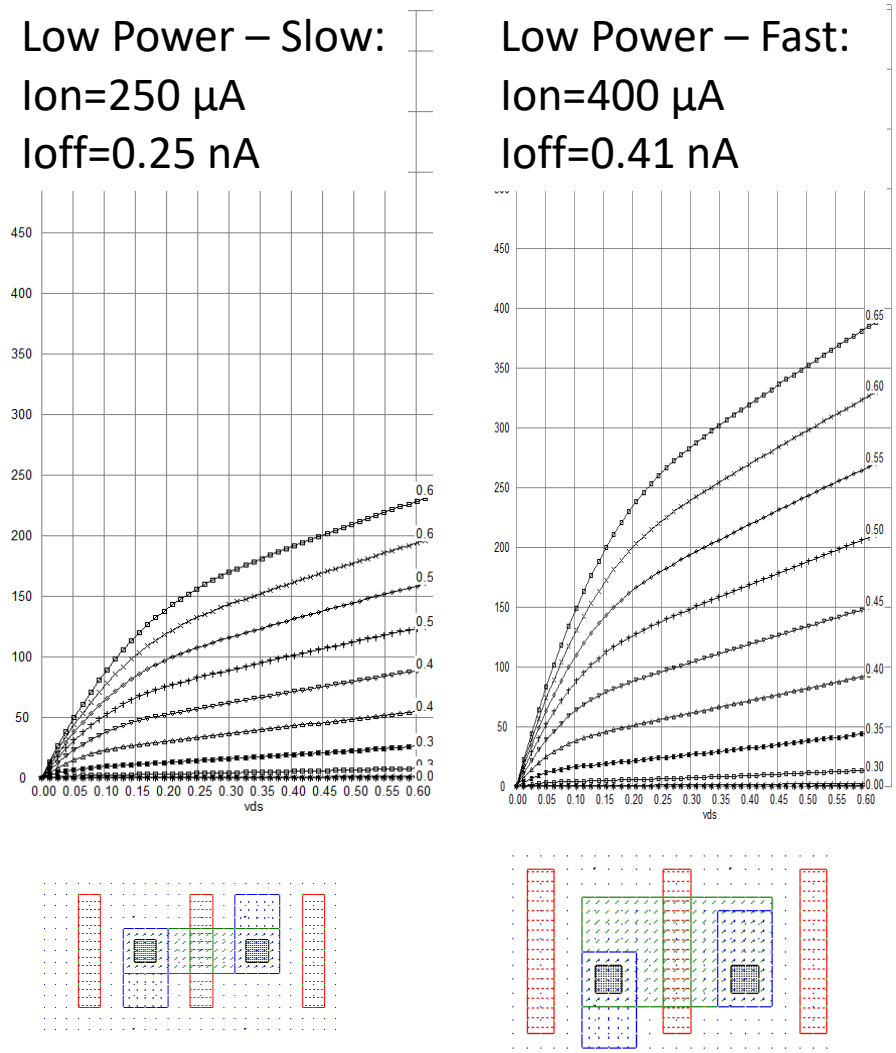
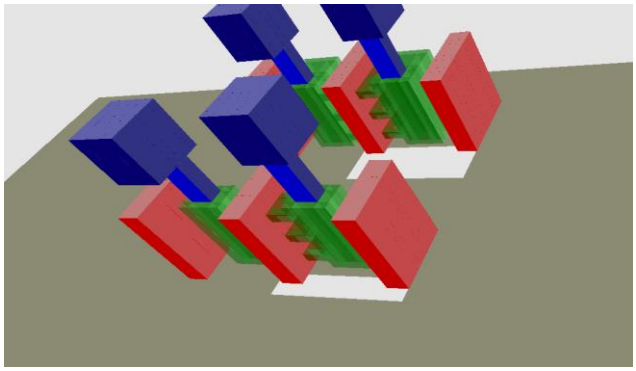


Figure 4.0 5 3D of NSFET



4.2 ALU Design

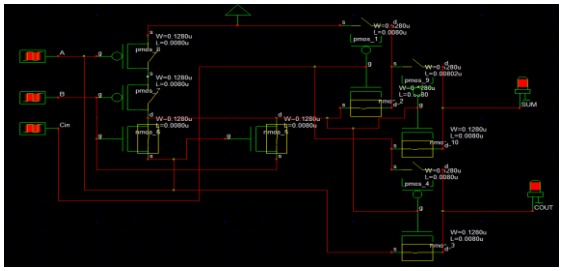
The design of a 8 bit ALU considered here is assumed to perform five functions that include two basic arithmetic operations such as Addition, Subtraction and three logic operations such as AND,OR and NOT. Different transistor logics were employed for different functions based on the advantages offered by each logic families.

4.2.1 NSFET Based Eight Bit Full Adder/Subtracter

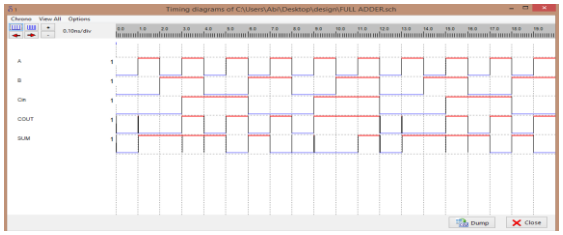
The very important part of the ALU which determine the overall performance of the design is the full adder for the arithmetic operations. Based on the procedures discussed in chapter 3 the design of 8 bit full adder/subtracter was performed as follows. First the function of 1 bit full adder was discussed with truth table, schematic, timing and layout diagram. According to figure 4.6 a) the total number of transistor is 10 and among them 5 is P-type and 5 is N-type NSFET and there are 3 inputs (A, B, Cin) and two outputs (SUM and Cout). As the above figure show sum and carry is equal to logic one, while 3 inputs are logic one and this is the same as what we can observe from truth table. In the above figure b) show the timing diagram or wave form of proposed system and its result was compared with the value in table 4.1 and it indicates that the proposed system is working correctly without any mismatch with truth table.

Table 4.1 Truth Table of 1 bit Full Adder

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



a)



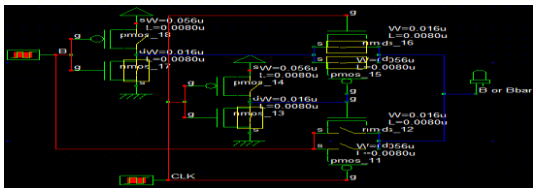
b)

Figure 4.0 6 Schematic and Timing Diagram of Proposed 1 Bit Full Adder

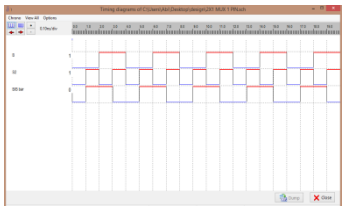
2X1 MUX

Table 4. 0 1 Truth table of 2x1 MUX

B	B bar	S2	Out put
0	1	0	B
1	0	1	B bar



a)



b)

Figure 4.7 Schematic and Timing Diagram of Proposed 2x1 MUX

The above figure 4.7 a) show that the total number of transistor is 8 NSFET and among them 4 is P-type and 4 is N-type. There are two inputs B and CLK, where B is normal input and CLK is selection or control signal and B or B bar is the output. The above figure 4.8 show the physical design of proposed 2x1 MUX which was generated automatically by compiling Verilog code in Microwind 3.9 and the Verilog code was explained in Appendix B. the width and length of the layout is 1 and 0.5 µm respectively therefore the total surface area of the layout is 0.5 μm^2 and total number of transistor is 8 (4 P-type and 4 N-type). According to the figure 4.9 a) the parasitic capacitance, resistance and inductance of output node is 1.1 fF, 3439 ohm and 2.2pH respectively. Figure b) was extracted from spice netlist which was converted from layout and it show the parasitic capacitance of all 6 nodes and according to spice netlist which was explained in Appendix A the output node ("BbBbar") refereed as node5 and its parasitic capacitance (C5) is 1.097fF which is approximately equal to 1.1fF. According to figure 4.10 a) the wave form of proposed system is very nice and the power consumption is around 4.89uw and the propagation delay (average of rise and fall delay) is 103.5ps.

According to figure b) the maximum operating frequency is 2.5 Gz which is very nice for multiplexer circuit. According to table 4.4 when power of proposed system is bad, other performance measure (delay, operating frequency and area are god or vice versa). Table 4.5 show that the proposed Adder / Subtracter circuit perform subtraction if and only if S_2 = C_{in} = high and Otherwise it perform Addition of A and B or A and B_{bar}. According to figure 4.11, the total number of transistor is 18, which means ten from full adder and 8 from 2x1 MUX (9 P-type and 9 N-type). There are 3 inputs (A, B, Cin), one control signal (CLK) which control addition and subtraction operation and two outputs (SUM and Cout).

Figure 4.0 7 Layout and Area of proposed 2x1 MUX

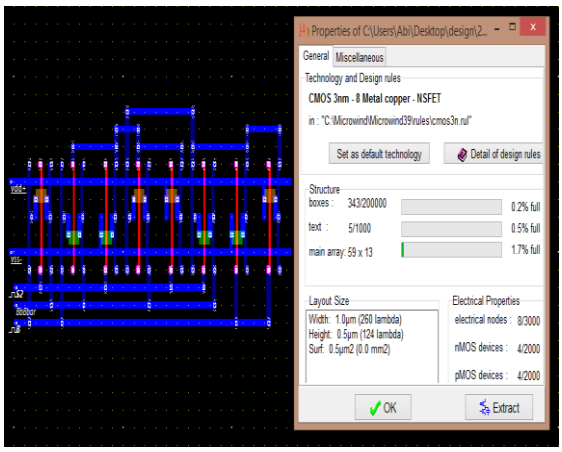
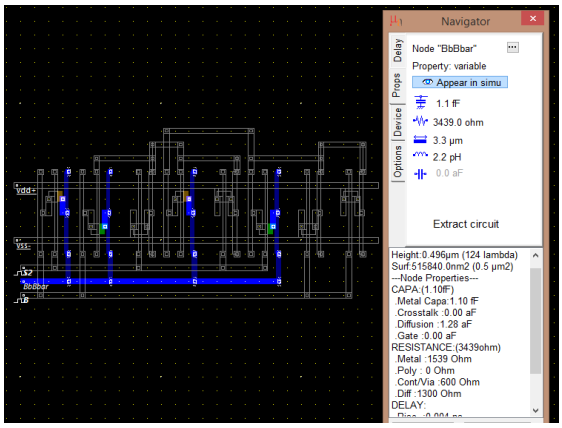


Figure 4.9 Parasitic Parameter Extraction

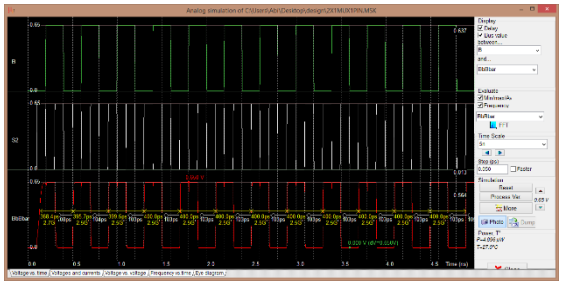


a) From layout

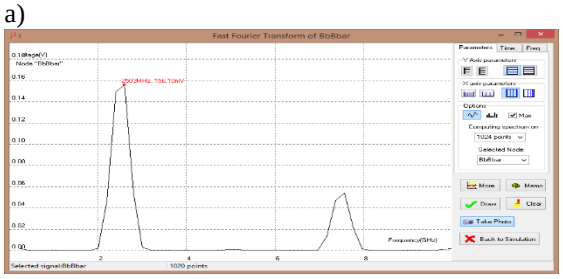
```
Spice File :C:\Users\Abi\Desktop\design\2X1MUX1PIN.CIR
* "BbBbar" corresponds to no5
* "B" corresponds to no6
* "S2" corresponds to no8
*
* MOS devices
MN1 0 6 2 0 N1  W=0.224U L=0.008U
MN2 2 8 5 0 N1  W=0.224U L=0.008U
MN3 0 8 4 0 N1  W=0.224U L=0.008U
MN4 6 4 5 0 N1  W=0.224U L=0.008U
MP1 1 6 2 1 P1  W=0.224U L=0.008U
MP2 1 8 4 1 P1  W=0.224U L=0.008U
MP3 2 4 5 1 P1  W=0.224U L=0.008U
MP4 6 8 5 1 P1  W=0.224U L=0.008U
*
C2 2 0  1.025fF
C3 1 0  0.406fF
C4 4 0  0.733fF
C5 5 0  1.097fF
C6 6 0  0.892fF
C8 8 0  0.540fF
*
*
* n-MOS BSIM4 :
* Low leakage, SVT
.MODEL N1 NMOS LEVEL=14 VTHO=0.300 U0=0.021 TOXE= 1.1E-9 LINT=0.000U
+K1 =0.700 K2=0.000 DVT0=1.300
+DVT1=0.500 LPE0=1.200e-9 ETA0=0.080
+NFACTOR=  1.1 UA=6.500e-15
+WINT=0.000U UC=-0.047e-15 PSCBE1=500.000e6
+KT1=-0.060 UTE=-1.800
+XJ=0.150U NDEP=170.000e15 PCLM=1.100
+VSAT=100000.000 VOFF=0.000
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p
```

b) From spice netlist

Figure 4.0 8 Result of Post Layout Simulation with Maximum Operating Frequency



a)



b)

Table 4.0 2 Performance Comparison of Existing and Proposed 2x1 MUX

Operation	power	Area	Delay	Parasitic parameters	Operating frequency
2x1 MUX [13]	**910.727 µW**	17.8ns	-	-	-
2x1 MUX [14]	**0µw**	**13.5 µm²(2T)**	-	-	-
2x1 MUX [30]	**0.61221µw**		-	-	-
2x1 MUX [proposed]	**4.896 µw**	**0.5 µm²(8T)**	**0.1035ns**	**3439 Ohm, 1.1Ff, 2.2pH**	2.5Gz

Table 4.0 3 Working Principle of Proposed Full Adder/Subtracter

S_2	C_{in}	A	B	SUM	Cout	Operations
0	0	0	0	0	0	A + B
0	1	0	1	0	1	A + B
1	0	1	0	0	1	A + B_{bar}
1	1	1	1	0	1	A+ B_{bar} +1

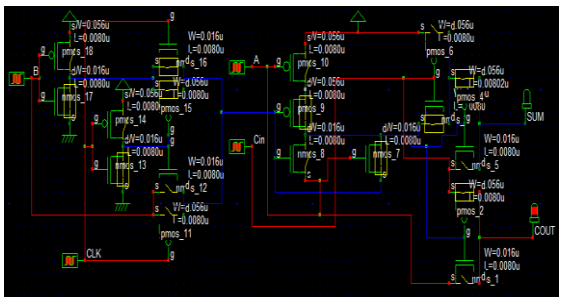
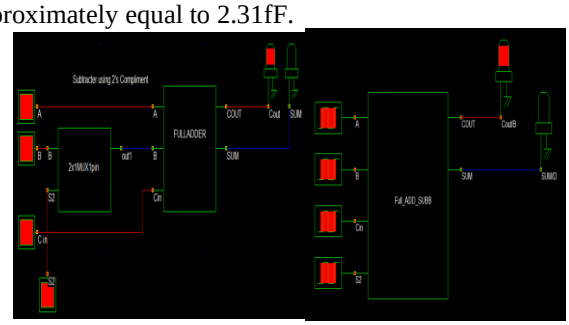


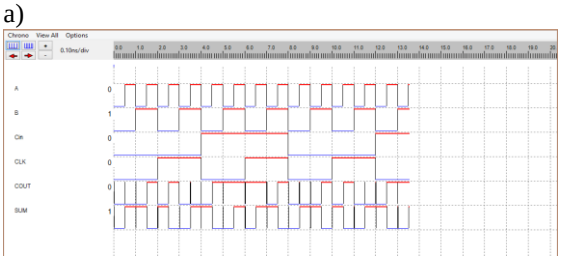
Figure 4.0 9 Schematic Diagram of Proposed 1 bit Full ADD/SUB

According to the figure 4.12 a) the single symbol which was converted from schematic diagram for sake of design simplicity and it has 6 pins (4 input and 2 output pins), 4 input pins are.

A, B, Cin and CLK (S2) and two output pins are SUM and Carry. Figure b) show the Timing diagram which was generated after schematic simulation and it clearly show that operating frequency of the system was 2.5 Gz or 0.4ns and the output of the simulation is exactly much the value in table 4.5. Figure 4.13 show the layout which was generated automatically from schematic and Appendix B explain the Verilog code which was used to generate this layout and the properties of layout show that the width, length and total surface area of layout is 2.2um, 0.7um and 1.5um^2 respectively and total number of transistor is 18 (9 N-type and 9 P-type). Figure 4.14 a) show the extraction process of parasitic parameters from layout and it indicates the parasitic capacitance, resistance, inductance, rise delay and fall delay of Sum node is 0.78fF, 2310 ohm, 0 nH, 0.003ns, 0.003ns respectively and Figure b) show the parasitic capacitance of 13 nodes which was obtained from spice netlist. According to the spice netlist explained in Appendix A., sum node is referred as node 10 and its parasitic capacitance is C_{10} =0.78fF. The figure 4.15 show the wave form of post layout simulation of proposed system and as we observe from the above waveform the output waveform doesn't move up and down properly, this is caused by some parasitic parameters like capacitance, resistance and inductance, which was discussed in figure 4.14. Although there are some parasitic parameters the output wave is very nice wave form and also above figure 4.15 show that the power consumption is around 2.925uw and temperature is 27^{0}c. The figure 4.16 below show that the proposed 8 bit ripple carry adder was designed by combining eight 1 bit full adder/subtracter and its functionality was verified according to table 4.7 and it is working without any violation. When one full adder/subtracter generate carry, it propagate to next and that is why we call it ripple carry adder/subtracter. The total number of transistor is 144(72 P-type and 72 N-type). Figure 4.17 show the schematic diagram of proposed 8 bit ripple carry adder/subtracter which was designed by using symbol of one bit full adder/subtracter and the total number of symbol of one bit full adder/subtracter is 8, carry out of one symbol is used as carry in to next symbol, which means carry is propagate from one symbol to another and that is why we call it as ripple carry adder/subtracter. 4 keyboard was used and each of them are 4 bit, the 1st two keyboard was used for $A_{0\text{-}3}$ and $B_{0\text{-}3}$, where the last two are used for $A_{4\text{-}7}$ and $B_{4\text{-}7}$. Each symbol has 6 pins, 4 input and 2 output pins, the single CLK or control signal was given to all symbol and the sum output of each symbol was connected with 8 bit display, where the carry of last symbol was taken as final carry out. According to the above. Figure 4.18 Physical design of 8 bit ripple carry adder/subtracter was done and it was designed automatically by using Verilog code which was explained in Appendix B. The total number of electrical nodes and transistors is 91 and 144(72 P-type and 72 N-Type) respectively. The width, height, and total surface area of physical design is 6.6um, 3.7um and 24.3um^2 respectively. Figure 4.19 a) show the value of parasitic capacitance, resistance, inductance of node SUM1 is 2.31fF, 3625ohm and 0nH respectively. Figure b) show the global delay analysis with RC information, for example the SUM1 node has 0.01ns delay, c=2.3fF and r 3625ohm. Figure c) was obtained from spice netlist which was explained in Appendix A, according to spice netlist of proposed 8 bit ripple carry adder, SUM1 corresponds to node 9, therefore parasitic capacitance of node SUM1 is c9=2.308fF which is approximately equal to 2.31fF.



a)



b)

Figure 4.0 10 Schematic to Symbol and Timing Diagram of Proposed Adder and Subtract

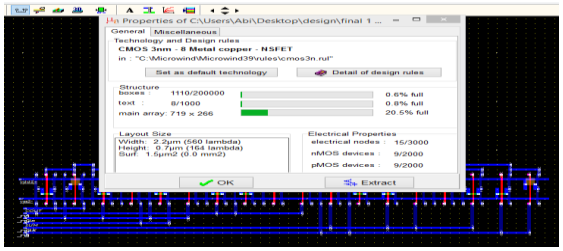


Figure 4.0 11 Layout Diagram of Proposed 1 bit Full Adder/Subtracter with its Area

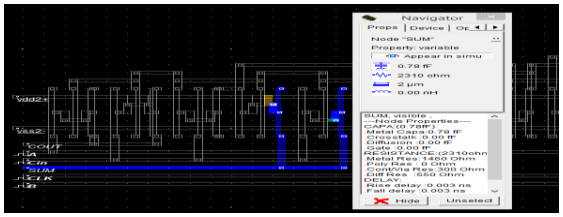
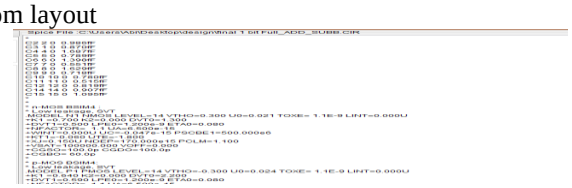


Figure 4.0 12 Parasitic Parameter Extraction

From layout



From spice netlist

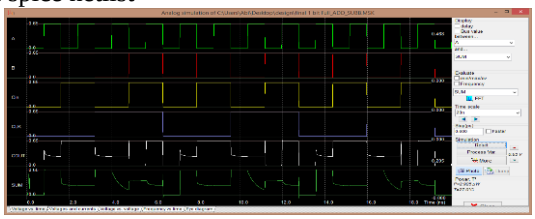


Figure 4.0 13 Wave form of Post Layout Simulation of Proposed 1 bit full Adder/Subtracter

Table 4.0 4 Performance Comparison Between Existing and Proposed full Adder/Subtractor

Operation	Power Consumption	Area (No. of Transistors)	Delay	Parasitic Parameter		
				Capacitance	Resistance	Inductance
ADD/SUB [1]	19.721nw	16T	8.942ps			
ADD/SUB [21]	581.542	8T	15.1311ps			
ADD/SUB [7]	9.004nw	22T	-			
ADD/SUB [16]	0.041nw/0.097nw	-	39.21ns/59.3ns			
ADD/SUB [22]	15.69nw		4.89ns			
ADD/SUB [23]	0.233nw	-	2.5ns			
ADD/SUB [13]	3.3991mw		78.7ns			
ADD/SUB [14]	1.85µw	60.6 μm^2(11T)				
ADD/SUB [24]	1.74nw/ 1.53mw		7.83/2.87ns			
ADD/SUB [25]	0.5495 µw		74.52ps			
ADD/SUB [26]	60.67 µw	60T				
ADD/SUB [27]	-	478.06 μm^2 (28T)	3.795ns			
ADD/SUB [28] 70/180nm technology	0.075/0.156 µw	-	0.127/0.169ns			
ADD/SUB [29]	0.2285mw	10T	2.76s			
ADD/SUB [proposed]	2.925µw	1.5 μm^2 (18T)	3ps	0.78fF	2310ohm	0nH

Table 4. 0 5 Working Principle of Proposed 8 bit full Adder/Subtracter

S_2	C_{in}	Operations
0	0	Addition (A + B)
0	1	Addition (A + B)
1	0	Addition (A + B_{bar})
1	1	Subtraction (A+ B_{bar} +1)

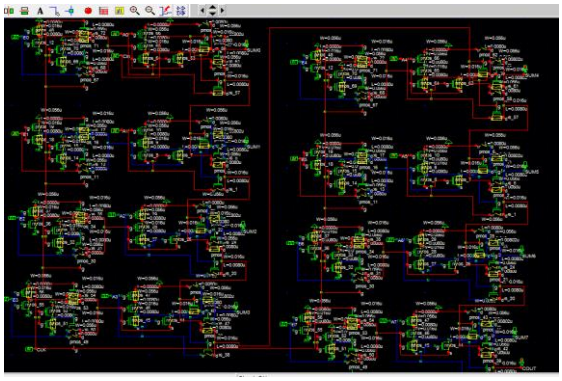


Figure 4.0 14 Schematic Diagram of Proposed 8 bit full Adder/ Subtracter.

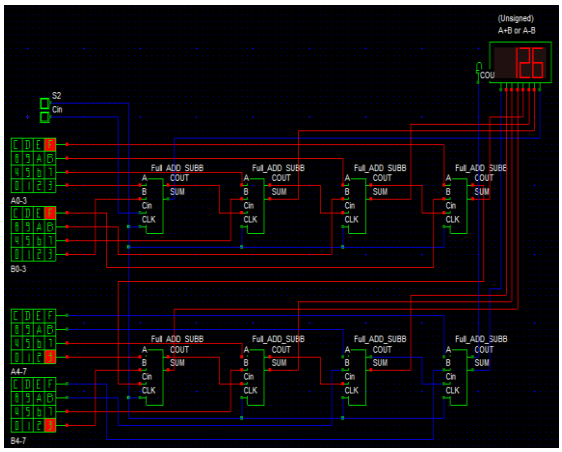


Figure 4.0 15 Schematic Diagram of Proposed 8 bit Ripple Carry Adder/Subtracter by using Symbol

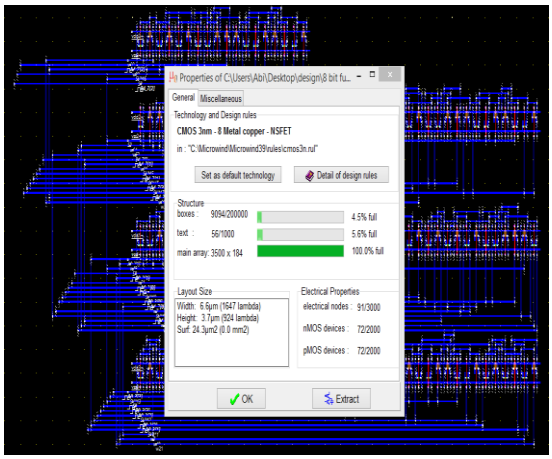
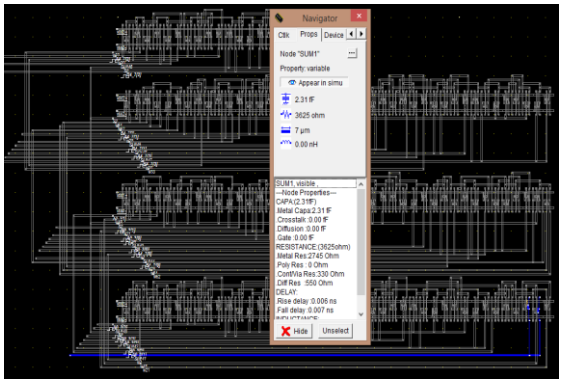


Figure 4.0 16 Layout Diagram of Proposed 8 bit Ripple carry Adder/Subtracter



a) From layout

Retrieval Number:100.1/ijvlsid.A1212033123
DOI:10.54105/ijvlsid.A1212.092222
Journal Website: www.ijvlsi.latticescipub.com

Published By:
Lattice Science Publication (LSP)

```
Microwind Version 3.9
RC information
C:\Users\Abi\Desktop\design\8 bit full adder-subtracter.MSK
generated on 9/17/2022, 3:28:13 AM
> 0.025ns, "w48", c=5.0fF, r=13079ohm
> 0.021ns, "w21", c=4.8fF, r=10249ohm
> 0.021ns, "w64", c=3.8fF, r=8316ohm
> 0.021ns, "w62", c=5.0fF, r=10822ohm
> 0.019ns, "w28", c=4.5fF, r=9835ohm
> 0.018ns, "w33", c=4.3fF, r=9694ohm
> 0.016ns, "w7", c=4.1fF, r=9355ohm
> 0.013ns, "w30", c=3.4fF, r=8530ohm
> 0.012ns, "N32", c=3.0fF, r=10571ohm
> 0.012ns, "N67", c=3.0fF, r=10571ohm
> 0.012ns, "N21", c=3.0fF, r=10541ohm
> 0.011ns, "N53", c=2.9fF, r=10481ohm
> 0.011ns, "N12", c=2.9fF, r=10481ohm
> 0.011ns, "N65", c=2.9fF, r=10451ohm
> 0.011ns, "N42", c=2.9fF, r=10451ohm
> 0.010ns, "SUM1", c=2.3fF, r=3625ohm
> 0.010ns, "SUM4", c=2.3fF, r=3595ohm
> 0.010ns, "SUM7", c=2.2fF, r=3430ohm
> 0.009ns, "COUT", c=2.0fF, r=3205ohm
> 0.008ns, "N44", c=2.6fF, r=7474ohm
> 0.008ns, "N14", c=2.6fF, r=7474ohm

C2  2  0   1.177fF
C3  3  0   0.842fF
C4  1  0   3.474fF
C5  1  0   3.400fF
C6  6  0   4.612fF
C7  7  0   3.839fF
C8  8  0   0.574fF
C9  9  0   2.308fF
C10  1  0   3.400fF
C11  11  0   2.020fF
C12  12  0   2.084fF
```

a) From spice netlist

Figure 4.0 17 Parasitic Parameter Extraction from Proposed 8 bit Ripple Carry Adder/Subtracter

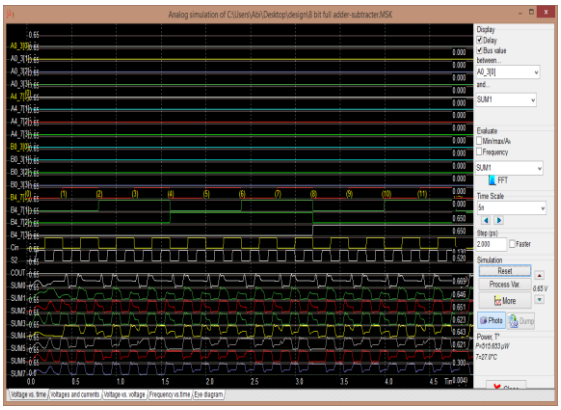


Figure 4.0 18 Post Layout Simulation Result of Proposed 8 bit Ripple Carry Adder/Subtracter

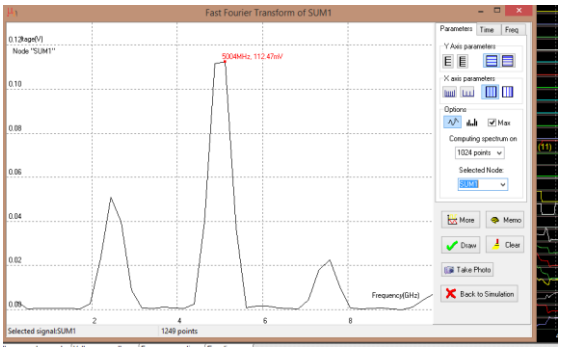
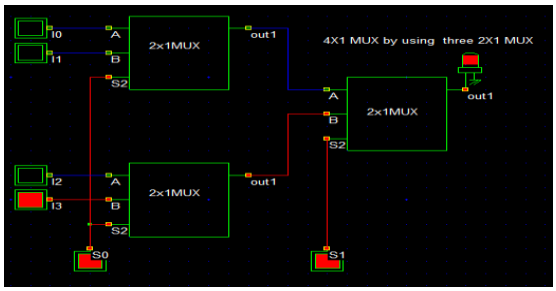


Figure 4.0 19 Maximum Operating Frequency of Proposed 8 bit Ripple Carry Adder/Subtracter

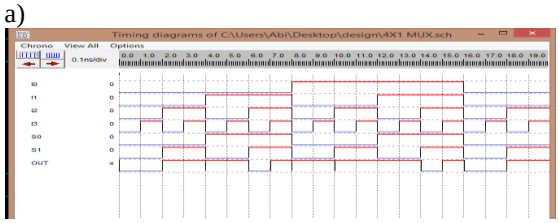
The above Figure 4.20 show the post layout simulation of proposed 8 bit ripple carry adder/subtracter and wave form is looks like very nice wave. The power consumption is around 515.65uw, which is little bit high because of NSFET and some parasitic parameters. However the power consumption of proposed system is little bit high, it has small area and high operating frequency. According to the figure 4.21 the maximum operating frequency of the proposed system is around 5004Mz (5.004Gz), which means the switching speed of the transistor is very nice and which is around 0.19ns, therefore the proposed adder/subtracter circuit compute the given operation at very high speed

4.2.2 4x1 MUX

Multiplexer is combinational circuit that used to select one among many inputs based on the selection line and we call it as data selector



a)



b)

Figure 4.0 20 Schematic and Timing diagram of 4x1 MUX

Table 4.0 6 Truth table of 4X1 MUX

S1	S0	Out put
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

As the above figure 4.22 a) show that the designer used three 2x1MUX to design one 4x1 MUX and each 2x1 Mux was designed by using 6 Fin type FET which is 7nm technology. Therefore the total number of transistor in proposed 4x1 Mux is 18 and it select one input among 4 input based on S0 and S1. Figure b) show that the proposed system is working properly as compare with truth table 4.8

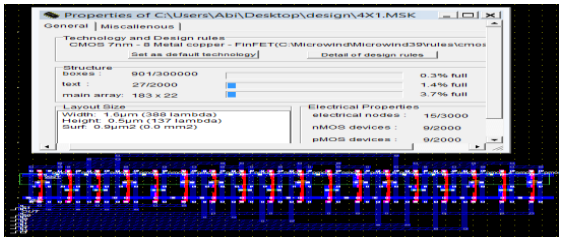
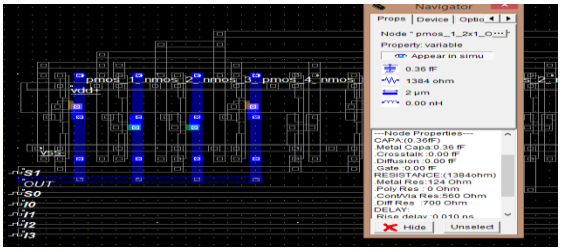
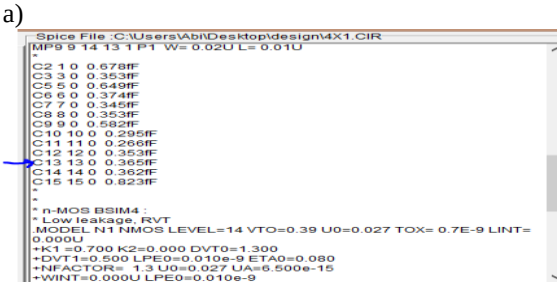


Figure 4.0 21 Layout Diagram of Proposed 4x1 Mux

Figure 4.23 show the physical design of proposed 4x1 MUX and it was generated automatically by using Verilog code which was explained in Appendix B and according to the layout there are 18 polysilicon layers in layout, therefore the total number of transistor is 18 (9 P-Type and 9 N-Type FinFET). The length and width of the layout is 0.5 and 1.6 µm respectively and area is 0.9µm^2.



a)



b)

Figure 4.0 22 Parasitic Parameter Extraction

Figure 4.24 a) show the parasitic parameters of output node and according to it the parasitic capacitance, resistance and inductance of output node is 0.36fF, 1384ohm and 0nH respectively. Figure b) show the parasitic capacitance of different nodes which was obtained from spice netlist of physical design and according to spice netlist which was explained in Appendix A the out node is corresponds to node 13 and the parasitic capacitance of node 13 is 0.36Ff.

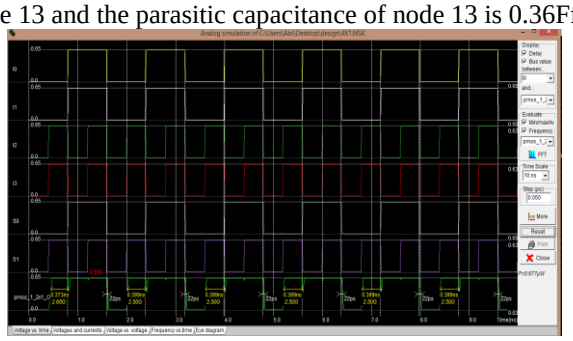


Figure 4.0 23 Post Layout Simulation Result

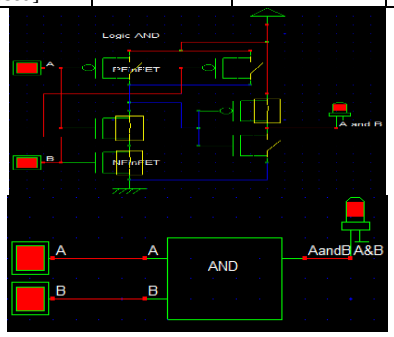
Figure 4.25 show the result of post layout simulation using BSIM4 and According to simulation result the total power consumption is 0.677uw, operating frequency is 2.5 Gz and propagation delay is 22ps.

4.2.4 Logic AND Gate Design

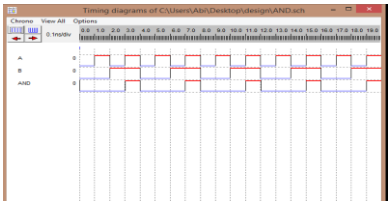
A researcher used static CMOS Logic to design AND gate and AND gate is given as Y =AB. Therefore it need two P-Type FinFET in pull up network and two N-Type FinFET in pull down network and finally one static FinFET inverter is needed. Below table 4.10 show the truth table of AND gate.

Table 4.0 7 Performance Comparison Between Existing and Proposed 4x1 Mux

Operation	Power	Area(No.of transistors)	Delay	Parasitic parameters			Frequency
				Resistance	Capacitance	Inductance	
4x1 MUX[13]	2.05mw		159.9ns				
4x1 MUX [14]	0Mw	39.4 μm^2(6T)	-				-
4x1 MUX [26]	330.5 Mw		-				-
4x1 MUX [proposed]	0.67 µw	0.9 μm^2(18T)	22ps	1384ohm	0.36fF	0.00nH	2.5 Gz



a)

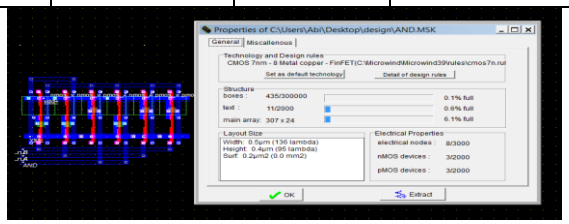


b)

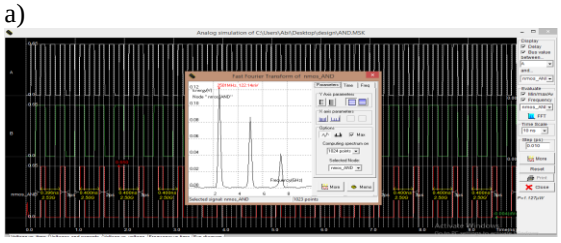
Figure 4.0 24 Schematic and Timing Diagram of Proposed AND Gate

Table 4.0 8 Truth table of AND gate

A	B	AND
0	0	0
0	1	0
1	0	0
1	1	1



a)



b)

Figure 4.0 25 Layout and Post Layout Simulation Resutlt of Proposed AND gate

Figure 4.26 a) show the schematic diagram of propsed AND gate which contain 6 tansistors, where 3 P-type was connected in pull up network and 3 N-type was connected in pull down network, figure b) show the schematic diagram of proposed AND gate was working correctly.

The above figure 4.27 a) show that the proposed AND gate was designed by using 6 Fin type FET(3 N-type and 3 P-type) and the length and width of the layout is 0.4 and 0.5um respectively, therefore surface area of layout is 0.2μm^2. Figure b) indicates that the power consumption is 0.9μw, the operating frequency is 2.5 Gz, and fall and rise delay is 2 and 3ps respectively, therefore the propagation delay is 2.5ps. The rise time at the output depends primarily on how fast the P channel device can turn on, and the fall time is determined primarily by how fast the N channel device can turn on.

4.2.5 OR Gate

The researcher used static CMOS logic to design OR gate and the equation Y = A + B. P-type in pull up network was connected series and N-type in pull down connected in parallel. Table 4.11 show the truth table of OR gate.

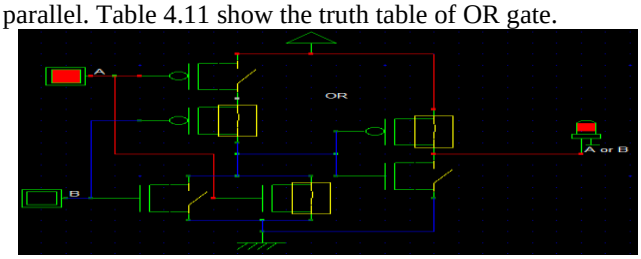


Figure 4.0 26 Schematic Diagram of Proposed OR Gate

Table 4.0 9 Truth Table of OR Gate

A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

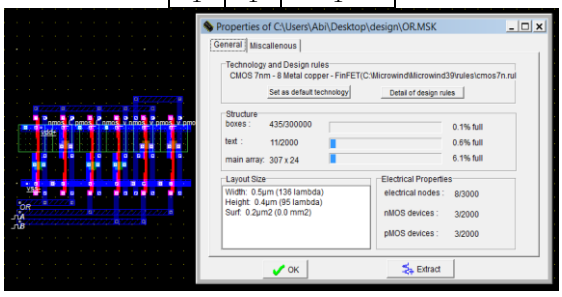


Figure 4.0 27 Layout of Proposed OR Gate

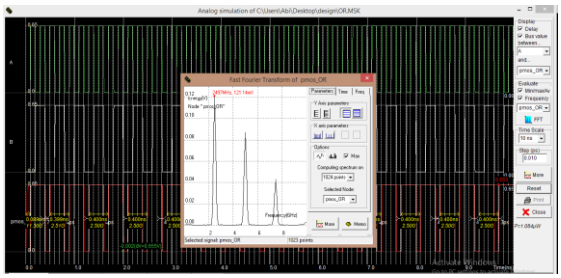


Figure 4.0 28 Post Layout Simulation Result

The above figure 4.28 show that proposed OR gate was designed from 6 transistors, where 3 P-type was connected in pull up and 3 N-type was connected in pull down network. Figure 4.29 show the physical design of proposed OR gate, which was generated automatically from Verilog code (Appendix B explain Verilog code) and the properties of the layout show the width, height and surface area which is 0.5um,0.4um and 0.2um^2 respectively, and it also show the electrical nodes, number of P-type and N-type transistor which is 8,3,3 respectively According to figure 4.30 the post layout simulation was done by using BSIM4 and it gives very nice result, wave form is exactly good, the power consumption is around 1.06uw, propagation delay is 3.5ps and the maximum operating frequency is 2.5Gz.

4.2.6 NOT Gate

The designer designed logic NOT gate by using CMOS technology and it has only two transistors (one at pull up and one at pull down network) and figure 4.15 show its schematic diagram and simulation result. Table 4.12 show the truth table of NOT gate.

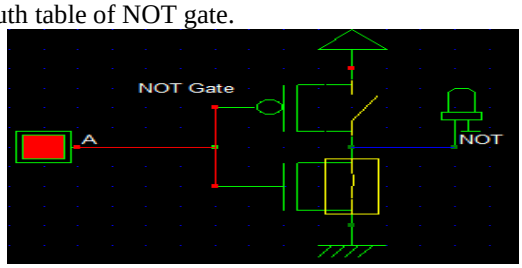
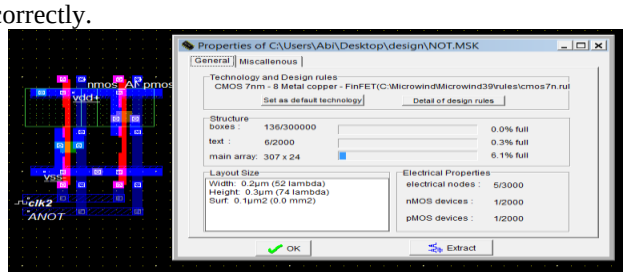


Figure 4.0 29 Schematic Diagram with Simulation Result of Proposed NOT Gate

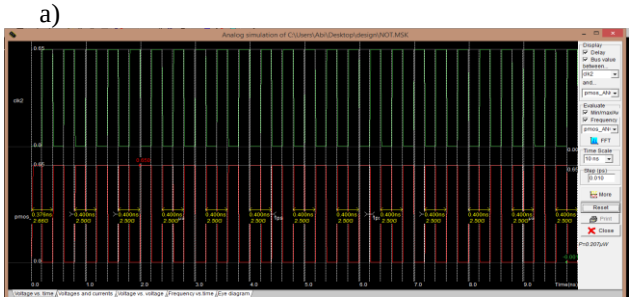
Table 4.0 10 Truth Table of NOT Gate

A	NOT
0	1
1	0

The above figure 4.31 show that the schematic of proposed NOT gate which was designed from 2 Fin Type FET and the simulation result indicates that the schematic was working correctly.



a)



b)

Figure 4.0 30 Layout of Proposed NOT Gate and it's Simulation Result

According to the above figure 4.32 a) the number of ploysilicon layer is only two which indicates that the total number of transistor in proposed design was 2, and there are two pins(one is input pin and the other is output pin). The length and width of the layout is 0.3 and 0.2μm respectivily, therefore the surace area of the layout is 0.1μm^2. Figure b) show the operating frequency, propagatin delay and power dissipation which is 2.5 Gz ,1ps and 0.2μw respectivily.

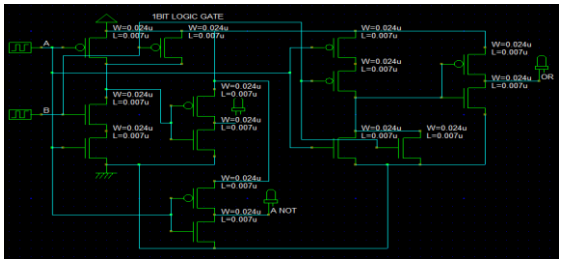


Figure 4.0 31 Schematic Diagram of Proposed 1bit Logic Gates

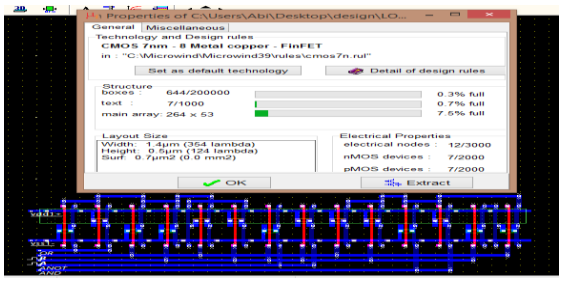
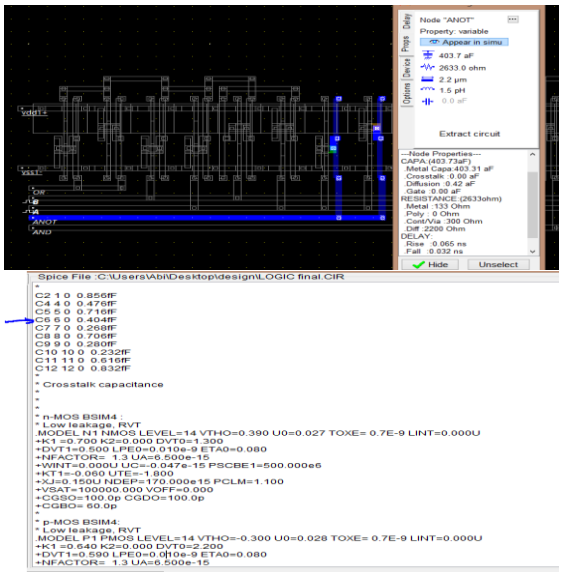
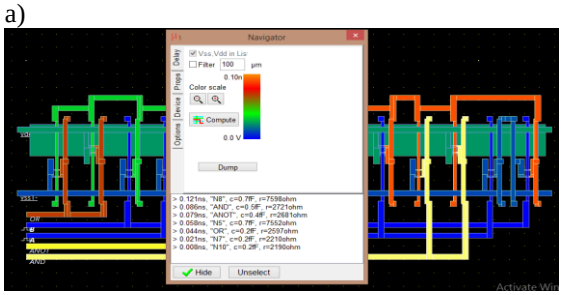


Figure 4.0 32 Layout Diagram of Proposed 1 bit Logic Gates



a)



b)

Figure 4.0 33 Parasitic Parameter Extaction and Global Delay Analysis

According to figure 4.33 the schematic diagram of proposed 1 bit logic gates has 14 transistors, 6 for AND, 6 for OR and 2 for NOT gate and it show that the schematic diagram of proposed one bit logic gates are working correctlly. Figure 4.34 Show the pysical design of proposed one bit logic gates, which was generated automatically by using verilog code(Appendix B explian this verilog code). According to the layout diagram the width, hieght and surface area is 1.4um,0.5um and 0.7um^2 respectivly. According to figure 4.35 a) the parasitic parameter of NOT node was extracted and it gives parasitic capacitance, resitsnce and inductance values which is 403.7fF, 2633ohm, 15pH respectivly. It also show the parasitic capacitance of different nodes that extracted from the spice netlist of pysical design.

Accordiing to spice netlist which was explianed in Appendix A, the NOT node is corosponds to node 6 and the parasitic capacitance of this node is C6= 0.404fF, figure b) show the result of global delay analysis which gives global delay and RC informatio of each node

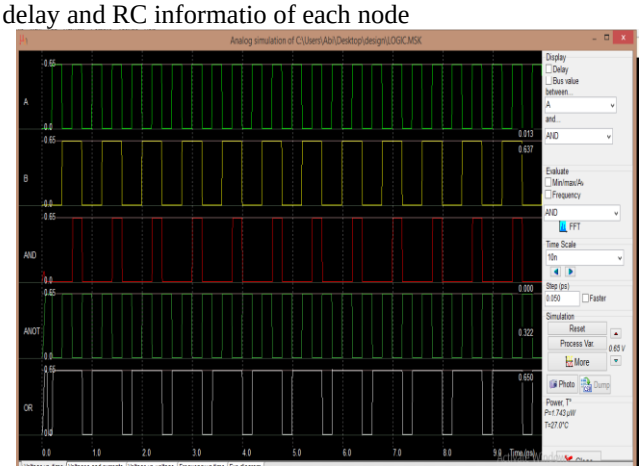


Figure 4.0 34 Post Layout Simulation Result

According to figure 4.36 the designer performed the post layout simulation after extracting spice netlist with parasitic parameters and the result show that all 3 logic gates are working properly and power consumption was 1.74uw.

Table 4.0 11 Performance Comparison Between Existing and Proposed Logic Gates

Operation	Power	Area /No of Transistors	Delay	Parasitic Parameters			Operating Frequency
				Capacitance	Resistance	Inductance	
AND [13]	533.939µw		38.46ns	-	-	-	-

AND [22]	12.48n		23.42ps	-	-	-	-
AND [24]	0.23mw		22.01ns		-	-	-
AND [29]	0.00126mw	2T	2.96s	-	-		
AND [26]	55.83 Mw	8T	-	-		-	
OR [13]	713.62 µW		38.1ns	-	-		-
OR [15]	0.1	-	0.99ns	-		-	-
OR [22]	14.36nw		597ps		-	-	-
OR [24]	0.215mw		5.09ns	-	-	-	-
OR [29]	0.0041mw	2T	1.16s	-	-	-	-
NOT [22]	2.26nw		4.99ps			-	-
NOT [13]			28.25ns		-	-	-
NOT [24]	0.117mw		12.1ps	-	-	-	-
NOT [26]	35.92 µW	8T	-			-	-
AND [proposed]	1.172µw	0.2 µm^2	2.5ps	0.5fF	2721ohm	-	2.5Gz
OR [proposed]	1.084µw	0.2 µm^2	3.5ps	0.2fF	2597ohm	-	2.5Gz
NOT [proposed]	0.207 µW	0.1 µm^2	1ps	0.4fF	2681ohm	15pH	2.5Gz

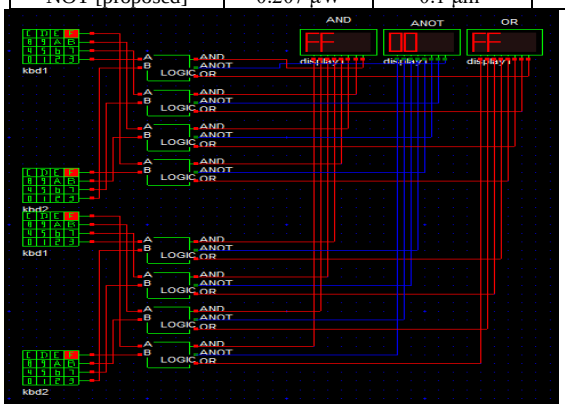


Figure 4.0 35 Schematic Diagram of Proposed 8 bit Logic Gates with Simulation Result

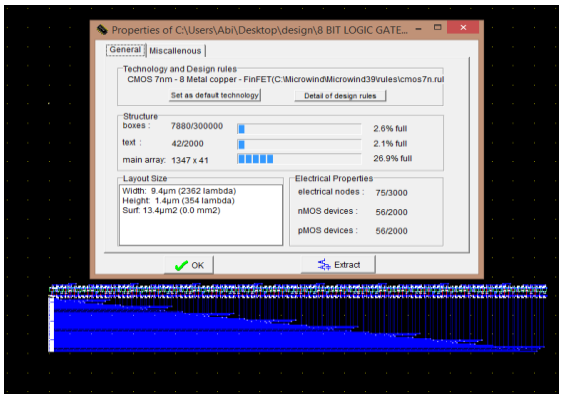
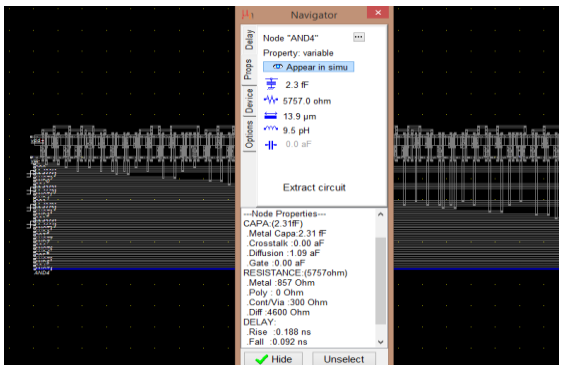


Figure 4.0 36 Layout Diagram of Proposed 8 bit Logic Gates



a) From layout

```
Microwind Version 3.9
RC information
C:\Users\Abi\Desktop\design\LOG.MSK
generated on 9/19/2022, 8:57:11 AM
> 0.188ns, "AND4", c=2.3fF, r=5757ohm
> 0.182ns, "ANOT4", c=2.2fF, r=5729ohm
> 0.173ns, "OR4", c=2.1fF, r=5689ohm
> 0.167ns, "AND5", c=2.1fF, r=5661ohm
> 0.162ns, "ANOT5", c=2.0fF, r=5633ohm
> 0.153ns, "OR5", c=1.9fF, r=5593ohm
> 0.147ns, "AND6", c=1.8fF, r=5565ohm
> 0.141ns, "ANOT6", c=1.7fF, r=5537ohm
> 0.133ns, "OR6", c=1.6fF, r=5497ohm
> 0.127ns, "AND7", c=1.6fF, r=5469ohm
> 0.121ns, "ANOT7", c=1.5fF, r=5441ohm
> 0.113ns, "OR7", c=1.4fF, r=5401ohm
> 0.107ns, "AND3", c=1.3fF, r=5373ohm
> 0.101ns, "ANOT3", c=1.2fF, r=5345ohm
> 0.091ns, "OR3", c=1.1fF, r=5297ohm
> 0.085ns, "AND2", c=1.0fF, r=5269ohm
> 0.079ns, "ANOT2", c=1.0fF, r=5241ohm
> 0.077ns, "N26", c=0.9fF, r=11316ohm
> 0.077ns, "N44", c=0.9fF, r=11316ohm
> 0.077ns, "N50", c=0.9fF, r=11316ohm
> 0.077ns, "N38", c=0.9fF, r=11316ohm
```

b) From spice netlist

Figure 4.0 37 Paraistic Parameter Extraction

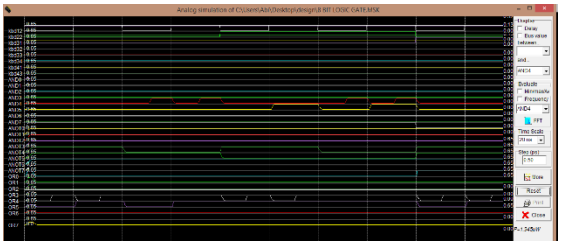


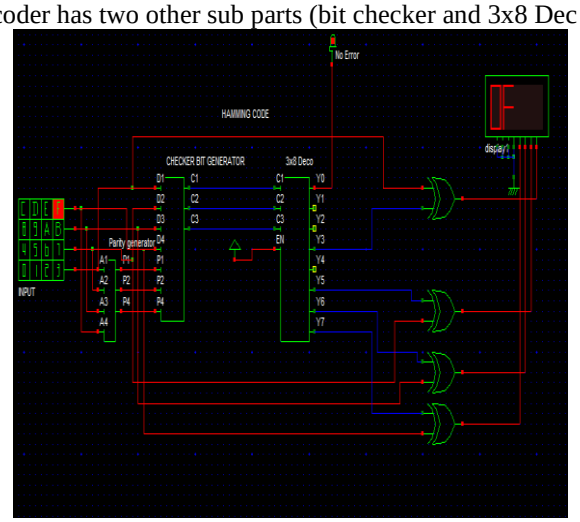
Figure 4.0 38 Post Layout Simulation Result

Figure 4.37 show the schematic diagram of proposed 8 bit logic gates and its simulation result. It show that proposed 8 bit logic gates was designed by using eight one bit logic gates and it has 4 keyboard(each of them are 4 bit), three 8 bit display(one for AND, one for OR and one for NOT gate). It also show that the schematic of proposed 8 bit logic gates are working properly without any problem and according to it A= FF & B=FF, A and B is FF, A OR B is FF and A NOT is 0. Figure 4.38 a) show the physical design of proposed 8 bit logic gate and it was generated automatically by using Verilog code which was explained in Appendix B and according to the physical design the width, height and total surface area of layout is 9.4um, 1.4um and 13.4um^2 respectively. It also show the total number of electrical nodes is 75 and devices is 112(56 P-type and 56 N-type FinFET). According to figure 4.39 a) the parasitic capacitance, resistance and inductance of node AND4 is 2.3fF,5757ohm and 9.5pH respectively and figure b) show the result of global delay analysis and according to it the global delay and parasitic RC value of 70 electrical node was analyzed.

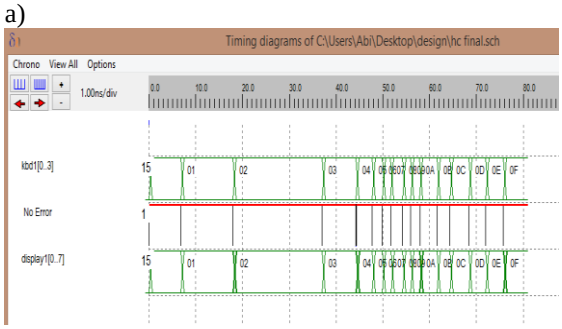
According to figure 4.40 the post layout simulation was done by using BSIM4 model and it gave very nice wave form with power consumption which is around 1.43uw.

4.3 Hamming Code Design

In this section Designer designed error detection and correction circuit by using (7,4) hamming code which has two main parts (hamming encoder which encodes data and hamming decoder which perform decoding function) and decoder has two other sub parts (bit checker and 3x8 Dec).



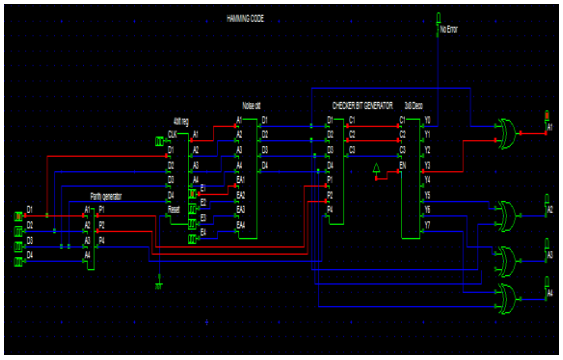
a)



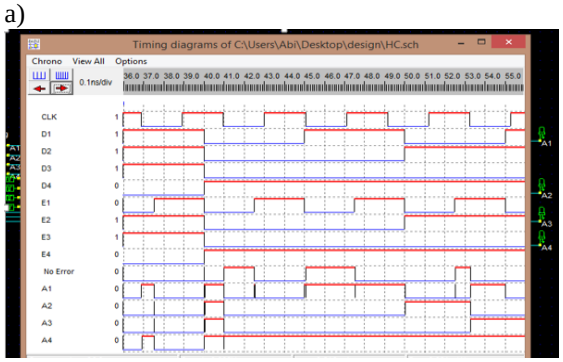
b)

Figure 4.0 39 Schematic and Timing Diagram of Proposed Hamming Code

Figure 4.41 a) show the schematic diagram of proposed hamming code which has two main parts hamming encoder and hamming decoder. Hamming encoder or parity bit generator consists 6 XOR gate which is used to generate parity bit (P1, P2 and P4). Decoder circuit of hamming code has two main components, one is checker bit generator and the other is 3x8 decoder. The check bit generator consists of 9 XOR gate and the inputs for checker bit generator are data and parity bits, the outputs are C1, C22 and C3. The inputs for decoder are the outputs of checker bit generator and the outputs are $Y_{0\text{-}7}$. Except Y_0 which is used to detect error, all are exored with corresponding data and parity bit. The 3x8 decoder in the above figure 4.37 has 4 input pins (C1, C2, C3 and CLK) and 8 output pins and it consists of 8 four pin AND gate and 3 NOT gate. Its working principle is almost the same as normal decoder. Figure b) show that the proposed hamming code is working properly.

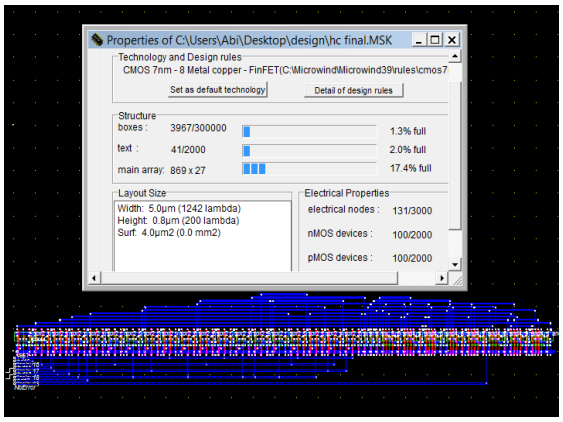


a)

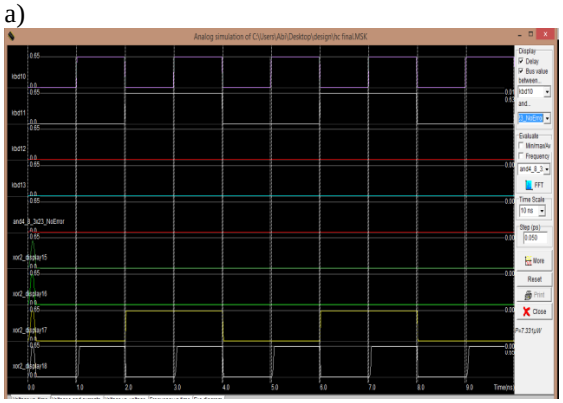


b)

Figure 4.0 40 Schematic and Timing Diagram of Hamming Code with Noise



a)



b)

Figure 4.0 41 Physical Design and Post Layout Simulation of Proposed Hamming Code

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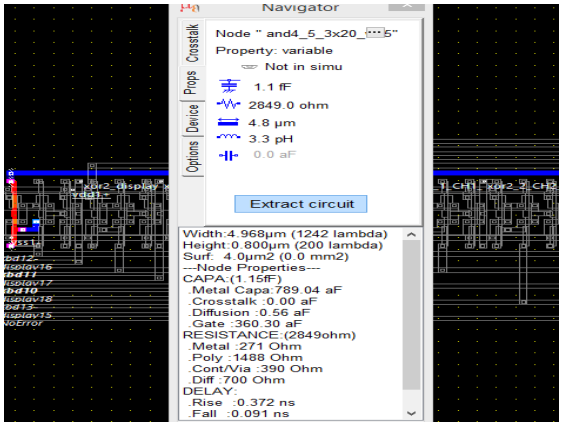


a) From layout

```
Microwind Version 3.9
RC information
C:\Users\Abi\Desktop\design\hc final.MSK
generated on 9/22/2022, 5:04:10 AM
> 0.964ns, " xor2_3_CH3_w14", c=3.0fF, r=11660ohm
> 0.919ns, " xor2_6_CH6_w12", c=2.8fF, r=10333ohm
> 0.913ns, " xor2_9_CH9_w13", c=2.8fF, r=11597ohm
> 0.721ns, " inv_2_3x17_w33", c=2.2fF, r=9924ohm
> 0.704ns, " inv_3_3x18_w34", c=2.2fF, r=8631ohm
> 0.695ns, " inv_1_3x16_w32", c=2.1fF, r=8622ohm
> 0.428ns, " and4_11_3x26_w16", c=1.3fF, r=2916ohm
> 0.390ns, " and4_9_3x24_w17", c=1.2fF, r=2653ohm
> 0.372ns, " and4_5_3x20_w15", c=1.1fF, r=2849ohm
> 0.348ns, " and4_4_3x19_w19", c=1.1fF, r=4090ohm
> 0.286ns, " xor2_2_Pa11_w11", c=0.9fF, r=3177ohm
> 0.285ns, " xor2_4_Pa13_w10", c=0.9fF, r=4015ohm
> 0.238ns, " xor2_5_Pa14_w30", c=0.7fF, r=3959ohm
> 0.235ns, " xor2_1_Pa10_w5", c=0.7fF, r=2685ohm
> 0.224ns, " xor2_3_Pa12_w29", c=0.7fF, r=3725ohm
> 0.214ns, " xor2_6_Pa15_w31", c=0.7fF, r=2660ohm
> 0.212ns, " and4_8_3x23_NoError", c=0.7fF, r=1002ohm
> 0.176ns, " xor2_8_CH8_w28", c=0.5fF, r=3887ohm
> 0.176ns, " xor2_7_CH7_w27", c=0.5fF, r=3887ohm
> 0.176ns, " xor2_2_CH2_w24", c=0.5fF, r=3887ohm
```

b) From spice netlist

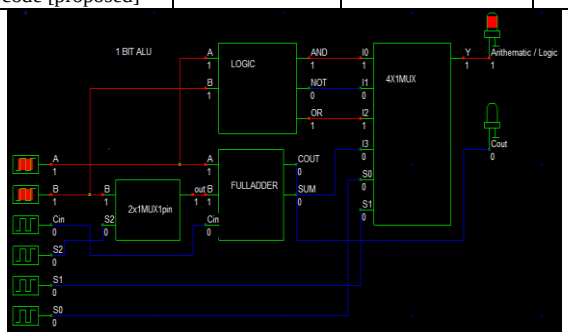
Figure 4.0 42 Parasitic Parameter Extraction

Figure 4.42 a) show that the researcher designed Noise circuit in order to check whether the proposed Hamming code detect and correct error or not and it show the overall schematic diagram of hamming code which is consists of Register, Noise, parity generator, check bit generator and 3x8 Decoder. As you have seen from the figure 4.38 a and b the hamming code work properly and it detected and corrected error (initially D1 is logic one but after passing Noise circuit it became logic zero, however the final D1 (A1) is the same as the initial D3). Figure 4.43 a) shows the physical design of proposed hamming code which was generated automatically by using Verilog code and this Verilog code was explained in Appendix B, according to the physical design the width, height and surface area of layout diagram is 5um, 0.8um and 4um^2 respectively. Figure b) show the post layout simulation results and according to it power consumption is around 7.7uw. Figure 4.44 a) show the parasitic capacitance, resistance and inductance of node "and4_5_3x20_w15" which is 1.1fF, 2849ohm and 3.3pH respectively. As figure b) indicates the global delay analysis was done and it gave value of global delay, parasitic RC of each nodes and among them the maximum delay, maximum capacitance and resistance is 0.96ns, 3fF and 11660ohm respectively.

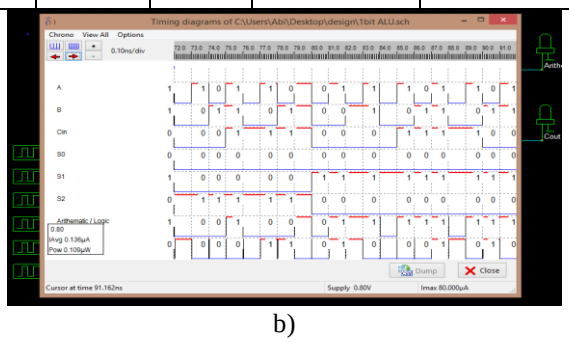
The design of four submodule was over and the next step is combining them together, therefore the designer combined them together as follows:- first 1 bit ALU was designed by combining already designed 1 bit full adder/subtracter, 1 bit logic gates and 4x1 MUX and here figure 4.45 below shows its schematic and timing diagram. Finally 8 bit ALU with and without error detection and correction code was designed by combining already designed 8 bit ripple carry adder/subtracter, 8 bit logic gates, 4x1 MUX and (7,4) hamming code and figure 4.46 below shows its schematic and timing diagram.

Table 4.0 12 Performance Comparison Between Existing and Proposed Hamming Code

Operation	Power Consumption	Area (No.of Transistors)	Technology	Delay	Parasitic Parameters		Operating Frequency
					C	R	
(7,4) Hamming code [30]	7.199 µW	-	90nm	0.99ns	-	-	
(7,4) Hamming code [31]	19 µW	36T	-	33.9ns	-	-	
(7,4) Hamming code [32]	3.271043w	-	16nm	-	-	-	-
(7,4) Hamming code [proposed]	7.33µW	4um^2	7nm	0.96ns	3fF	11660ohm	2.5 Gz



a)

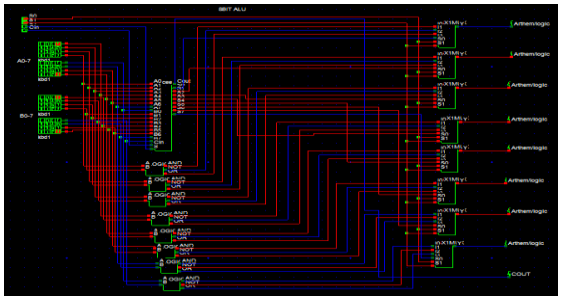


b)

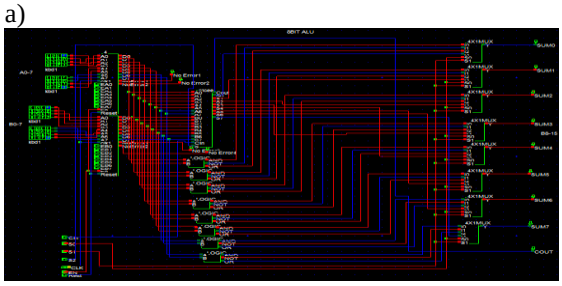
Figure 4.0 43 Schematic and Timing Diagram of Propsed 1 bit ALU

Table 4. 0 13 Performance Comparison Between Existing and Proposed 1bit ALU

Operation	Power	Area/ No of Transistors	Delay	Operating Frequency
1Bit ALU [33]	21.369µW	1190.95 μm^2(38)	17.8ns	-
1Bit ALU [24]	1.96mw	-	101.8ps	
1Bit ALU [34]-[47]	15.3mw	-	-	-
1Bit ALU [15]	24µw	-	4.49ns	-
1Bit ALU [proposed]	0.109µw	2.9μm^2(area of 1 bit full ADD/SUBB + area of 1 bit logic gate+ area of 4x1 MUX)		2.5 Gz



a)



a)

Figure 4.0 44 Schematic Diagram and Simulation Result of Proposed 8 bit ALU with and without Hamming Code

The above figure 4.46 a) show that schematic and simulation of proposed 8 bit ALU without error detection and correction code and figure b) shows the proposed 8 bit ALU with error detection and correction code at input side and both figure a) and b) shows the addition of two 8 bits (A = 00111111, B = 00111111) and sum = 01111110, Cout =0. The proposed ALU consists of 8 bit Ripple Carry Adder circuit to perform both addition and subtraction, and 8 bit AND gate, 8 bit OR gate, 8 bit NOT gate, four (7,4) hamming code, four 4 bit registers, eight 4x1 MUX. The above table 4.16 a) shows the working principle of proposed ALU with error detection and correction code at input side and table b) shows the proposed ALU without error detection and correction code.

Table 4.0 14 Working Principle of Proposed 8bit ALU with and Without Error Detection and Correction Code

Clk	rst	En	Cin	S_2	S_1	S_0	Operations
1	0	1	x	0	0	0	AND
1	0	1	x	0	0	1	OR
1	0	1	x	0	1	0	NOT
1	0	1	x	0	1	1	Addition
1	0	1	1	1	1	1	Subtraction

a)

Cin	S_2	S_1	S_0	Operations
x	0	0	0	AND
x	0	0	1	OR
x	0	1	0	NOT
x	0	1	1	Addition
1	1	1	1	Subtraction

b)

Table 4.0 15 Performance Measure of Proposed ALU with and Without Hamming Code

Operation	Power	Area	No. of error detected	No. of error corrected
ALU with HC	(515.653+1.345+0.67+7.7) µw =525.36 µw	(24.3+13.4+0.9+4)µm^2 = 42.6 μm^2	8	4

a)

Operation	Power	Area
ALU without HC	(515.653+1.345+0.67) µw =517.66 µw	(24.3+13.4+0.9)μm^2 = 38.6 μm^2

b)

V. SUMMARY AND CONCLUSION

5.1 Introduction

In this chapter the designer summarized and concluded his overall design and finally explained the future works or recommendations.

5.2 Summary

The designer designed smart 8 bit ALU with and without error detection and correction at input side by using so many steps. The first step was decomposing the proposed circuit in to 4 main parts (Arithmetic, logic, multiplexer and hamming code part) and design each part separately by using producers discussed in chapter 3 and different technology (3nm technology for Arithmetic part and 7nm technology for Logic, Multiplexer and Hamming code part) and physical or layout design and schematic diagram of all 4 modules was designed by using MICROWIND 3.9 and DSCH 3.9 software respectively. At the end of each module design, schematic diagram simulation, parasitic parameter extraction, global delay analysis and post layout simulation was done and finally performance of each module was measured and compared with existing design in terms of Area, number of transistors, power consumption, propagation delay and operating frequency. After completing each part design, interface of Arithmetic, logic and multiplexer was done to get proposed ALU without error detection and correction at input side and performance was measured in terms of Area and power consumption and also interface of Arithmetic, logic, multiplexer and hamming code was done to get proposed ALU with error detection and correction at input side and its performance was measured in terms of Area, power consumption and number of error detected and corrected.

5.3 Conclusion

According to table 4.4 the performance measure of proposed system was calculated and compared with existing system and also the power consumption of proposed 2x1 MUX was decreased from 910.727uw to 4.896uw, propagation delay was decreased from 17,8ns to 0.103ns, area was decreased from 13.5um^2 to 0.5um^2. According to figure 4.10 post layout simulation was done and even though there are some parasitic parameters, the wave form result of post layout was very smooth. According to table 4.6 the power consumption of proposed 1 bit full adder/subtracter is decreased from 3.3991mw to 2.925uw, delay decreased from 78.7ns to 3ps and area was decreased from 478.06 um^2 to 1.5 um^2. As figure 4.15 show, the physical design of proposed 1 bit full adder/subtracter was simulated and even though there are some parasitic parameters, the wave form of post layout simulation is so smooth this is due to novel NSFET. According to figure 4.18 the width, height and total surface area of proposed 8 bit Ripple Carry Adder/Subtracter was measured and their values are 6.6um, 3.7um and 24.3um^2 respectively. It also indicates that the number of electrical node is 91 and total number of transistor is 144(72 P-type and 72 N-type). As figure 4.20 and 21 shown the power consumption of proposed 8 bit ripple Carry Adder/Subtracter was 515.65uw, which is little bit high because of 3nm Technology (as technology shrinks down the number of transistor is become high and this leads to high power consumption) and the operating frequency is 5004Mz (5.004Gz), which is very high and it means NSFET switch on and off at very high speed and due to this novel feature of NSFET, the designed ripple carry adder/subtracter compute the given operation with in friction of ns and it has very small area. As shown in figure 4.20, the designer performed post layout simulation and got very nice result, even though there are some parasitic parameters. As shown in table 4.13, the performance of logic gates was measured and compared with different existing system in terms of power consumption, area, propagation delay and operating frequency, and as it shown the result of proposed logic gate is very nice in many directions. According to table 4.15 performance of proposed 1bit ALU was measured and compared with existing system in terms of power consumption, Area, operating frequency and propagation delay. As shown in figure 4.46, the designed smart 8 bit ALU with and without error detection and correction code was working correctly and its performance was measured in terms of area, power consumption, number of error detected and number of error corrected, which was shown in table 4.17.

5.4 Future Works

Due to lack of time and other challenges, I have some works that I had planned to do in future, one of them is using NSFET to design all modules in order to reduce total area of proposed chip, and implement some adiabatic circuit to reduce power consumption which occurs when technology shrinks down from 7nm to 3nm. In proposed system Error detection and correction code was implemented only at input side, in future I will implement at output side also and will try to implement other error detection and correction code like reed-Solomon code and if it is possible I will try to develop deep learning to detect and correct fault in proposed system and design control part of CPU.

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Authors Contributions	I am only the sole author in this article.

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