Indian Journal of VLSI Design (IJVLSID)
ISSN: 2582-8843 (Online), Volume-2 Issue-1, March 2022

# Analysis of Velocity Measurement of Radar Signal in Space Vehicle Application using VLSI Chip

**E. N. Ganesh**

***Abstract:*** ***The objective of the project is to design a low cost Spectral Monitor for a Space vehicle velocity measurement application, based on Doppler Shift principle by generating an radar signal source from earth station towards moving target device in space and processing received high speed analog 200MHz radar signal from target vehicle device through Antenna, analog pre-processing and FPGA based spectral analyzer. The hardware reconfigurable spectral analyzer design consist of ADC(500MSPS) Interface block, SRAM Memory(1024x16) block, Radix-2 FFT (16 bit DSP block) and LCD Display (Monitoring) driver algorithm implemented On-Chip SOC-FPGA system. The proposed algorithm can be used to meet the need of many real time application such as space exploration, wideband communication, command and control application. The desired algorithm is implemented on-chip reconfigurable hardware SOC-FPGA while keeping the cost, power and area of device low compared to general purpose processor and Embedded based microcontroller. The code architecture is described using hardware description language, VHDL and synthesized and simulated using Xilinx 12.2 ISE Design suite.***

***Keywords: System on Chip (SOC), Field Programmable Gate Array (FPGA), Analog to Digital Conversion (ADC), Hardware Descriptive Language (HDL), Fast Fourier Transform (FFT).***

## I. INTRODUCTION

In many real time applications such as velocity measurement, medical diagnostic domain, space exploration, wide band communication, command communication and control, spectral analysis is needed for the purpose of monitoring, surveillance and/or control. The proposed module algorithm can be implemented on software , hardware based architecture according to the desired specification and requirement. The software architecture based algorithm design is best when the performance of a system is not important and task execution speed slow while keeping cost of the proposed system cheaper with more flexibility .The hardware architecture based algorithm design is best for hard real time based application and faster performance or computation based systems where task execution is very fast but cost of system will be little bit costlier compared to software based architecture. In the proposed system design high speed spectral analyzer is used for hard real time application and higher performance. Therefore the hardware architecture based implementation of a proposed system design or functionality is better than software based architecture implementation to meet the desired performance requirement, however software based algorithm implementation fails to meet the faster performance requirement of a purposed system. There are different technology's available for hardware based architecture implementation such as ASIC (Application specific integrated circuit) and programmable logic devices (PLD). The design implementation based on ASIC hardware implementation consumes high Non-Recruiting Engineering (NRE) cost and more time to market for designing a desired prototype device and design implementation based on programmable logic device (PLD) consumes less time to market and low Non-Recruiting Engineering (NRE) cost for a designing of a desired prototype device [1].

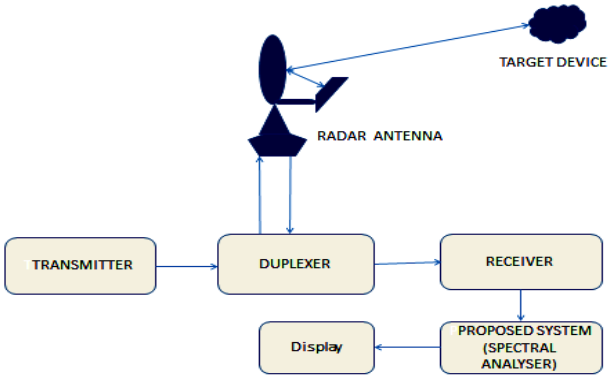


**Fig .1. Basic block of radar System**

In programmable logic based hardware implementation PAL, PLA, CPLD and FPGA based different technology available for hardware based design implementation [1]. In each of these technologies the internal hardware block architecture is different. The synthesized RTL code[2] of a design implementation on Programmable Array Logic(PAL) and Programmable Logical Array(PLA) based hardware architecture is similar technology to EPROM, allowing them to be programmed, erased using ultraviolet light and subsequently reprogrammed. On modern CPLD is programmed differently, Rather than using EPROM technology they use SRAM cells to store configuration bits. Initially configuration data stored in non-volatile flash RAM memory within CPLD chip is transferred to SRAM memory cells when power is applied.

**Manuscript received on 03 February 2022 | Revised Manuscript received on 11 March 2022 | Manuscript Accepted on 15 March 2022 | Manuscript published on 30 March 2022.**
***** Correspondence Author
**Dr. E. N. Ganesh***, Department of Electronics & Communication Engineering, Vels University, Chennai, (Tamil Nadu), India.

The design implementation on FPGA similar to CPLD technology but hardware designing complexity more on FPGA based hardware architecture compared to CPLD based hardware architecture [3]. In this project hardware reconfigurable based FPGA technology implementation is used for meeting the required functionality performance of the proposed design. Many sophisticated Spectral analysis devices are exist in the market based on Computer based (General purpose processor) and embedded microcontroller based system but these kind of system consumes more power, NRE cost, area and time to market. As well these kinds of systems have fixed hardware architecture, slower data acquisition speed and non-availability of sufficient on chip memory. In order to achieve faster performance compared to general proposed processor and embedded based microcontroller the proposed design is implemented on SOC-FPGA. In the proposed system the main objective is to measure velocity of moving target in space, by transmitting source radar analog signal from earth station to target device and processing received Doppler shift radar analog signal through antenna, analog pre-processing module and proposed design of spectral analyzer system SOC-FPGA to measure spectral (Frequency) of received analog signal. Based on the measurement of frequency parameter of a received analog radar signal through the spectral analyzer the velocity calculation of target device is performed. In this project work RTL Level design of Spectral analyzer done using VHDL language including 16 bit Dual port SRAM , 16 bit Radix-2 DIF FFT processing block, Power spectral Density calculation and LCD driver algorithm Synthesized and verified using Xilinx 12.2 IDE CAD tool.In the proposed system spectral analyzer is designed for calculating the frequency of received analog radar signal with on-chip radar signal processing [4]. The electronic principle of sound wave reflection is very similar to the principle of radar signal reflection. If we shout in the air in the direction of a reflecting object, we will hear an echo. Based on the measurement of time required for an echo to return can be roughly converted to distance based on speed of sound. Radar system also works much the same way with the help of electromagnetic energy as shown in below fig 1.1. The Radio Frequency (RF) signal transmitted towards the object and a small portion of reflected RF energy returns to radar set. This returned energy is called as echo. Based on returned echo signal radar set determine the direction and distance of reflecting object. The acronym of radar is made up of the words Radio Detecting and Ranging. Thus the radar set detects the presence of object by receiving the reflected RF energy. In the proposed system back scattering methodology used is the term given to reflection in the opposite direction to the incident rays [5]. Usually all target produce a diffusion reflection i.e. it is reflected in a wide number of directions also called as scattering. The basic blocks of primary radar explained as follows.

### A. Transmitter

The radar system transmits the short duration high power radio frequency signal pulses of energy into space by menace of antenna towards the targeted object to measure the velocity of target object.

### B. Duplexer

The duplexer is used to switch the antenna alternatively between transmitter and receiver.so at a time only one transmitter or receiver module will be active. This switching essential because high energy RF pulses of transmitter would destroy the receiver if energy allowed entering into the receiver.

### C. Receiver

The receiver receives the shot pulses of reflected echo signal from target object based on back scattering principle. The receiver amplifies the received weak signal and demodulates. The output of receiver is converted to digital samples and processing of digital samples takes place according to desired functionality.

### D. Radar Antenna

The antenna acts as a trans-receiver module, during transmission mode transfers the transmitter energy signal in space with required distribution and efficiency similar way it receives the reflected echo signal from target object with required distribution and efficiency .The duplexer is used to switch alternatively between transmitter and receiver.

### E. Spectral Analyser

The received reflected back scattered analog echo signal converted to digital samples, these digitalized samples processed through the Fast Fourier transformation technique to analyse the spectrum (frequency) of input signal.

### F. Display

In proposed system LCD display module is used to present user a continues, easily understandable, graphic information of the relative frequency of a reflected radar signal from a target device, for calculating velocity of radar targets. Radar system is used to measure the distance, direction, height and speed of these objects.

In the proposed system spectral analyser for radar signal is used for calculating the velocity of target object in space based on calculation of reflected echo signal frequency. The radar system is unaffected by darkness, fog and cloud. This permits the radar system to identify the position of airplanes, ships or other obstacle that are invisible to naked eyes because of long distance, bad weather and darkness

## II. EXISTING TECHNOLOGY DESIGN

Existing Spectral monitor system design classified into based on Computer based, microcontroller based and reconfigurable hardware.

### A. General propose based system

In computer based or general purpose processor based Spectral monitor design data received from external ports like parallel port, universal serial bus and it requires special cables to connecting and it increase the cost of device. The received data is processed through the software based fixed architecture processor and memory by performing data manipulation, visualization and/or decision making.

This computer based architecture obviously has the disadvantages of high cost, low speed and higher power consumption[6].

### B. Embedded based systems

The second spectral monitor based design is embedded system based microcontroller design. These kinds of designs are having advantages in higher performance and portability but having disadvantages in insufficient memory, low speed and fixed architecture. For example if present or existing microcontroller consist of 16 bit data width of 64 Kbytes SRAM memory and 128 Kbytes ROM memory but there are situation to improve the performance of system by increasing data width of 32 bit, SRAM memory size of 8192 Kbytes and ROM of 1024 Kbytes in this case it is mandatory to replace whole embedded system with new one by increasing cost of device.

### C. Hardware reconfigurable FPGA based

The existing hardware reconfigurable (FPGA) based Spectral analyser is designed for processing low frequency signal for biomedical and medical signal processing application with low sampling frequency and low data rate reading and writing the samples in SRAM memory with serial synchronous interfacing protocol between FPGA and ADC Data converter[7][8]. In the proposed system design the interface between the high speed ADC data converter with sampling frequency 500 MHz and FPGA is achieved based on parallel Low Voltage Ddifferential Ssignalling standards (LVDS).The parallel LVDS interface in the proposed system has the advantage over serial interface because it eliminates the serializing and de-serializing block at the input output block of FPGA internal architecture with high speed data transmission from master to slave. The high speed parallel data samples from ADC data converter directly stored in 16 bit SRAM memory block of FPGA with clock speed of 2ns. The stored sample data processed through Radix-2 DIF FFT Processing block[9] and Real and Imaginary output values of Radix-2 DIF-FFT processor is saved in SRAM memory block and power spectral density calculation performed on stored samples

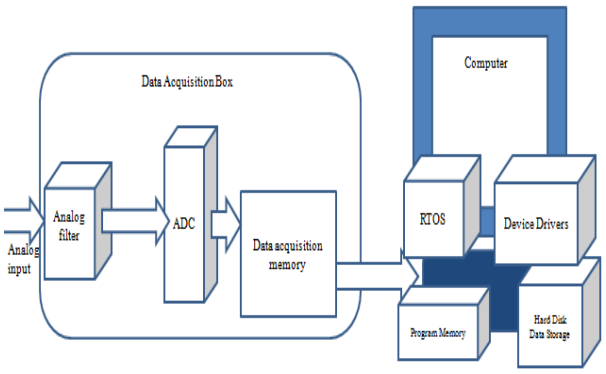


**Fig.2. Computer Based spectral analyser**

## III. PROPOSED SYSTEM SPECIFICATION AND DESIGN.

The proposed system is designed for the fallowing Specifications of Maximum input frequency of signal is 200MHz with a resolution of 500 KHz. The Sampling frequency of data converter is 500MHz and 1024 point FFT computation is performed. High speed Spectral analyser system comprises of High Speed ADC interfaced to a Field Programmable Gate Array (FPGA). The main components involved in the system are High Speed ADC, Level translators, SRAM, FPGA and LCD Display. Control logic unit implemented in the FPGA controls and coordinates the action of the various devices involved in data acquisition system. Interfacing between field programmable gate arrays (FPGA) and high speed ADC data converter is always an engineering challenge. In market many on-chip synchronous serial interfacing techniques are available such as SPI, I2C and JESD204. In serial interfacing technique the high speed data transmitted serially from master (Data converter) to slave (FPGA) and at slave region the high speed serial data converted to parallel data with the help of serialize and de-serialize .The output of de-serialized parallel data processed through the processing blocks to achieve desired functionality. In the proposed module design the interface between the high speed ADC data converter with sampling frequency 500 MHz and FPGA is achieved based on parallel Low Voltage Differential Signaling standards (LVDS).The parallel LVDS interface in the proposed system has the advantage over serial interface because it eliminates the serializing and de-serializing block at the input output block of FPGA internal architecture with high speed data transmission from master to slave. The high speed parallel data samples from ADC data stored in 16 bit SRAM memory block of FPGA with clock speed of 2ns. The stored sample data processing takes through Radix-2 DIF-FFT Processing block. The Real and Imaginary output values of Radix-2 DIF-FFT processor is saved in SRAM memory block and power spectral density calculation performed on stored samples. The module of proposed design explained as follow.

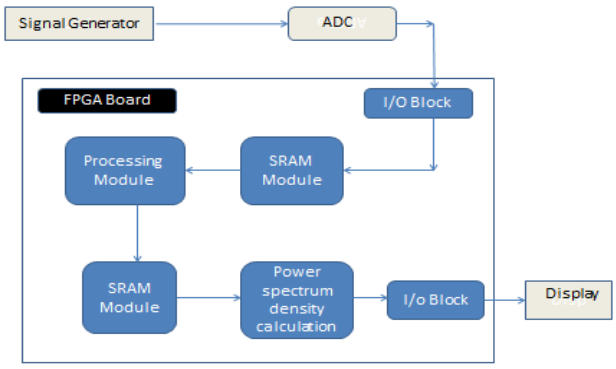


**Fig. 1. Proposed Module block Diagram**

ADC Interface : The Analog to digital converter used is ADS5463 an 80-pin IC which is a high speed ADC[9]. It has 12 – bit resolution with 500MSPS sample rate, whose outputs are LVDS compatible and has 2GHz input bandwidth. This is used for data acquisition, and ADS5463 is low noise and linearity over a large input frequency range. 2) On Chip SRAM : The ADC samples are stored in the (16x1024) on-chip SRAM with high speed data rate of 2ns and later samples will be accessed and FFT will be performed using FPGA DSP core with less execution speed as desired speed of 200 ns.

The On-chip SRAM module used as buffer in order to converting the high speed real time discrete signal to discrete frequency sample data.The high speed data synchronization and data writing rate are the main challenges while configuring SRAM module On FPGA chip..

*3) Processor:* In the proposed system 16 bit fixed point 1024 point Radix-2 DIF-FFT processor is used for digital signal processing application for converting real discrete time domain signal $X_n$ to discrete Fourier samples $X_k$. In the proposed system Radix-2, 1024 point DIF-FFT processing techniques is used for faster computation and performance by consuming less execution cycles for computing the multiplication operation compared to Discrete Fourier transformer because of symmetry and periodicity property of Fast Fourier transformation[10][11].

*4) Display:* In the proposed system LCD display module is used to present user a continues, easily understandable, graphic information of the relative frequency of a reflected radar signal from a target device, for calculating velocity of radar targets.

**TABLE I. Comparison of FFT Simulation Results in Matlab and Xilinx Software Tool**

| Index | Matlab FFT Simulation | | Xilinx FFT Simulation | |
|---|---|---|---|---|
| | Xk(Real) | Xk(Img) | Xk(Real) | Xk(Img) |
| 0 | 14272 | 0 | 14272 | 0 |
| 9 | 2302.668 | 2554.9 | 2302 | 2554 |
| 25 | 3841.332 | 250.8999 | 3841 | 250 |
| 32 | 0 | 0 | 0 | 0 |

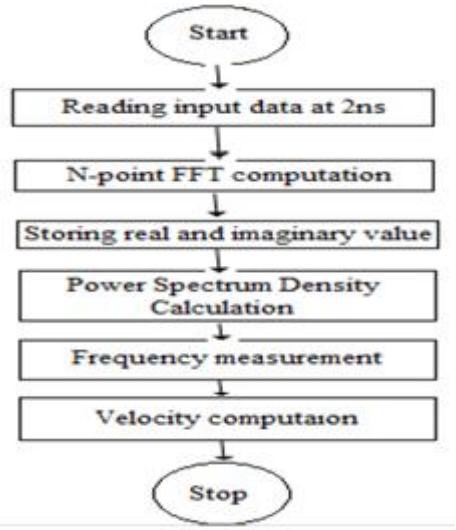


**Fig.4. Flowchart of velocity computation**

ADC samples will be stored in Memory and later samples will be accessed and FFT will be computed by DSP core of FPGA. The entire process involved in this system is explained using a flowchart shown in Fig .4. Based on the frequency measurement of an output signal of a Spectral analyser, the velocity calculation of target object takes place based on fallowing formulae.

$V = \lambda fd / 2$

where, V = Velocity

$\lambda$ = RF source wavelength

*f*d = Doppler frequency shift

## IV. PROPOSED SYSTEM SETUP, VERIFICATION RESULTS AND COMPARISON

### A. Proposed System Verification Results

In the proposed system memory design functional and place and route simulation verified using Xilinx Synthesis and Modelsim simulation tool and results are shown in table- 1.


**Fig.5.Data Reading to Memory at 500 MHz .**

The computation of DIF-FFT algorithm is verified using both Matlab simulation and Xilinx synthesis tool simulation. Matlab power spectrum density simulation result shown in the fig.6. and the Xilinx synthesis tool power spectrum density simulation result is shown in the fig.7.for the given 64 bit input lookup-table text file. The result shows the Matlab FFT

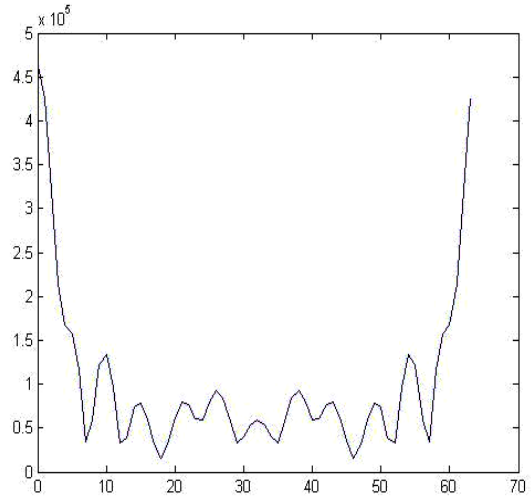


**Fig.6. Power Spectral Density Calculation in Matlab**

algorithm computation result matches with the Xilinx FFT Module synthesis Result.

### B. Proposed System Setup

A signal generator is used to generate 500 KHz to 200 MHz sine waves as input to the spectral analyser device. To validate the implemented methodology, several verification technique were performed using Matlab and Xilinx simulation tool.

The developed FPGA prototype has 16 – bit resolution with 500MSPS sample rate ADC, whose outputs are LVDS compatible and has 2GHz input bandwidth.

### C. Performance Evaluation

The proposed system works in a stand-alone mode without the need of computer or microprocessor.
All the processing and control done on a Stan-alone hardware re-configurable FPGA with concurrent execution of tasks with higher performance or faster computation compared to other proposed systems like computer based processor and embedded systems, in these systems task execution will be in sequential way with less computation speed.

### D. Cost Comparison

Using the current market value, The proposed system consist FPGA, LCD and ADC instrument. These instrument cost is less compared to other proposed systems based on micro-processor and Embedded based microcontroller .

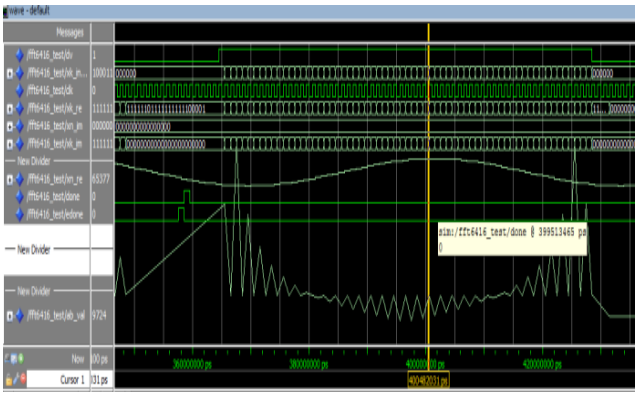

**Fig.7. Power spectrum density Calculation in Xilinx**

## V. CONCLUSION AND FUTURE SCOPE

In this paper, the conceptual design of a low-cost stand-alone Spectral analyser device has been provided. The instrument is universal, which means it can be employed in various areas such as wideband communications and medical, environmental, and radar applications. In applications where sampling rates are greater than 2 GS/s, such as wideband multichannel communication, the significance of the proposed instrument increases.

## REFERENCES

1. W. Wolf, FPGA-Based System Design. Englewood Cliffs, Prentice-Hall, 2004
2. S. Palnitkar, HDL, A Guide to Digital Design and Synthesis, Englewood Cliffs, NJ: Prentice-Hall, 1996.
3. XST User Guide for CPLD and Virtex-4, Sparten-3E, and 3A Series FPGA Devices. http://www.xilinx.com/support/documentation.
4. Drain, L.E. (1980) The Laser Doppler Technique, John Wiley & Sons,ISBN0-471-27627-8.
5. Basic principle of Radar System. URL: http://en.wikipedia.org/wiki/radarsystems..
6. S. Martin, “PC-based data acquisition in an industrial environment,” in Proc. IEE Colloq. PC-Based instrum., 2002,pp.2/1-2/3.
7. K. Arshak, A. Arshak, E. Jafer, D. Waldern, J. Harris ,“Low-power wireless smart data acquisition system for monitoring pressure in medical application,” Microelectron. Int., vol. 25, no.1.pp. 3-14, 2008. [CrossRef]
8. T. Lin and Z. Zhengou, “The implementation of 100 MHZ data acquisition based on FPGA,” in Proc.3rd IEEE Int. Workshop Syst. on-Chip Real Time Appl., Aug.2005, pp.241-246.
9. ADS5463 12-bit Resolution ADC. URL: www.dataconverter.ti.com.
10. U.M-Baese. Digital Signal Processing With Field Programmable Gate Arrays, Springer, 2007.
11. B. Baas, “A Low-power,high-performance,1024-point FFT processor,” IEEE Journal of solid-state Circuites,vol.34,no,pp.380-387,1999. [CrossRef]
12. Modelsim Manual Mentor Graphics Corporation. http://support.xilinx.com.
13. M. Abdallah, O. Elkeelany, and A. Alouani, “An efficient hardware reconfigurable multi-channel audio data acquisition, storing and monitoring system, ”in Proc.ICCE,2009,pp.1-2. [CrossRef]

## AUTHORS PROFILE

**I am Dr. E. N. Ganesh**, having 24 years of Teaching Experience out of which 8 years as Principal and 3 years as Dean at present. I am a M.Tech Graduate from IIT Madras in Microelectronics and VLSI Design, and PhD from JNTU Hyderabad in Nanotechnology with Gold Medal. I have Executed 6 Funded Projects with 5 patents granted. 5 More Patents are Published and all of them are in final evaluation stage. DST STTP Sponsored Funded one Crore project is in progress and at final stage to be submitted. I am Guiding 13 PhD students, 5 from Anna University and all of them awarded degree. I am having 48 Scopus indexed International Journals and 15 SCI Journals (Annexure I) with total 160 Publications to my credits. I have executed 12 Consultancy Projects for the cost of 60 Lakhs. I have more than 60 International Conference Publications. Twenty best Conference paper awards with Distinguish Faculty, Researcher and Excellence in teaching awards, reviewer and editor for 8 International Journals with four books Published (one International Publication.