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A Comparative Analysis of Gain and Bandwidth of CMOS Transimpedance Amplifier

Vineeta Singh, Sarika Parihar, Vandana Niranjan

Abstract: ***The paper presents the various trans-impedance amplifier (TIA) topologies has been studied and presented with an insight of their Gain and Bandwidth. The device parameters such as gain and bandwidth has been studied and compared for various TIA topologies. The performance of the presented topologies of TIA has been compared and summarized to get an overview. The comparison is done on the basis of its topology and device technology along with gain, bandwidth and power supply. In this paper recent advancement and future scope are also discussed.***

Keywords: ***Trans-Impedance Amplifier (Tia), Topology, High Gain, Bandwidth.***

I. INTRODUCTION

In recent years where many type of signals are used to convey the information such as optical signal in optical communication system, thermal rays etc. which compel us to study optical communications system. This TIA has many applications other than the optical fiber communication such as in automobile, Radio frequency and instruments used in medical etc. At receiver side this TIA is placed first which plays a major role for entire receiver system in terms of performance [20], consist of a photodiode for converting the light signal into a current carrying electrical signal which is further converted into amplified voltage signal. Transimpedance amplifier are needed to provide large bandwidth, high gain along with low power consumption[19].There are some issue in TIA as well such as Noise which is of main concern that should be taken care off while designing[32]. A transimpedance amplifier is basically a current-to-voltage converter and the ratio between its input current and its output voltage is called transimpedance, Z_{tr} is often characterized as transimpedance gain, given by following equation:

$$Z_{tr} = \frac{V_{out}}{I_{in}} \quad (1)$$

The paper is organized as follow: Section I. gives a basic idea about transimpedance amplifier (TIA) and its importance. Further, section II. In this various CMOS transimpedance amplifier (TIA) topologies are presented, in section III provides a discussion on the recent advancement. Section IV includes future scope and comparative study of parameters like gain and bandwidth along with topology and technology node used for various transimpedance amplifier.

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* Correspondence Author

Vineeta Singh*, Dept of Electronics &Communication Engineering, Indira Gandhi Delhi Technical University, for Women New Delhi, India. E-mail. Vineeta1009@gmail.com

Sarika Parihar, Dept of Electronics &Communication Engineering, Indira Gandhi Delhi Technical University, for Women New Delhi, India

Vandana Niranjan, Dept of Electronics &Communication Engineering, Indira Gandhi Delhi Technical University, for Women New Delhi, India

II. TIA TOPOLOGIES

For achieving various parameters such as Gain, Bandwidth etc. numerous configuration of TIA design has been shown.

A. Common source

In short (CS-TIA) topology a shunt-shunt feedback is used to reduce the input and output impedance. This CS-TIA is shown in figure.1 [26].In CS-TIA Topology, R_F is shunt feedback resistance, is used to give low input impedance. Resistive load (R_D), provides wideband response. Due to reduced input impedance this configuration will increase the bandwidth and provide high open loop gain [37] and reduced output impedance provides better driving capability. The sensitivity of common source TIA mainly depends on input node capacitance (C_{PD}), feedback resistor (R_F) and trans-conductance of input transistor. Trade-off between the gain and voltage is much more crucial for common source TIA because of Miller effect. This is one of the simplest configuration which is popularly used. Open loop Gain (A_{CS}) and BW of a common-source TIA are shown as: -

$$A_{CS} = -g_m R_O \quad (2)$$

Where, gm is the trans-conductance of M_n and R_O is the OL output resistance which is shown as:

$$Ro = \frac{R_D R_{DS}}{R_D + R_{DS}} \quad (3)$$

Here, R_D is drain resistance shown in figure.1. and R_{DS} drain to source resistance M_n. Bandwidth (BW) of a common source TIA is

$$BW = \frac{A+1}{2\pi(R_O + R_F)C_{in}} \quad (4)$$

C_{in} is the capacitance at input, addition of C_{PD} and Miller capacitance.

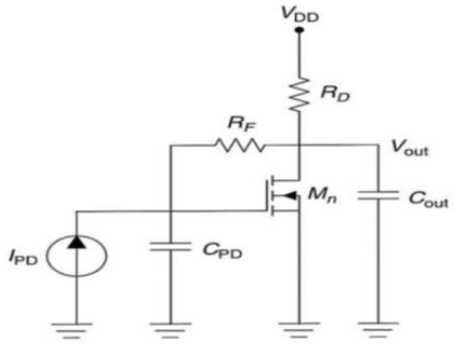

Fig-1: CS-TIA

B. Common gate

In short (CG-TIA) topology is also one of the simplest Trans-impedance amplifier topology presented in figure.2 [26] CG-TIA offers the low input impedance which in turn increases the bandwidth (BW) of the circuit along with low power consumption [30]. But at low supply voltages, noise is one of the main concern in common gate TIA topology. Its open loop Gain(A_{CG}) and Bandwidth (BW) are given below:

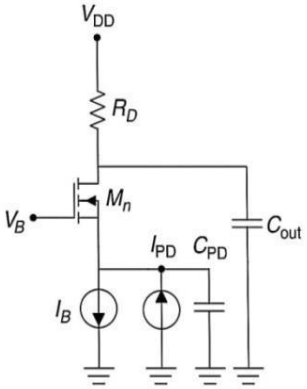

Fig-2: CG-TIA

Open loop gain (A_{CG}) of Common Gate topology as-

$$A_{CG} = -g_m R_O \quad (5)$$

Here, g_m is the transconductance of M_n and R_{out} is the output resistance.

Bandwidth of Common Gate TIA is

$$BW = \frac{g_m}{2\pi C_{pd}} \quad (6)$$

Here, C_{pd} is photodiode capacitance.

C. Regulated cascode TIA (RGC-TIA)

Topology which was earlier also known as common-gate TIA (CG-TIA) presented in figure. 3 [26]. This configuration offers less input impedance which provides high BW and less power consumption. Using the cascade structure in RGC topology, parasitic capacitance effect on bandwidth can be reduced. Here common source configuration MOSFET work as feedback for common gate configuration MOSFET, due to this the effective transconductance of whole circuit in increased thus the pole due to parasitic capacitance is isolated this leads to improved bandwidth.

The typical Regulated cascade amplifier suffers from the trade-off between the gain, bandwidth (BW) and input referred noise (I_N).

Voltage gain (A_{RG}) of M_{nrg} shown as

$$A_{RG} = -g_{mnrg}\frac{R_{DS}R_{rg}}{R_{DS}+R_{rg}} \quad (7)$$

Where g_{mnrg} is the transconductance of M_{nrg} and R_{rg} is the resistance of M_{nrg} (regulating amplifier)

And, BW of Regulated cascade Transimpedance amplifier is-

$$BW = \frac{g_{mn}}{2\pi C_{pd}} \quad (8)$$

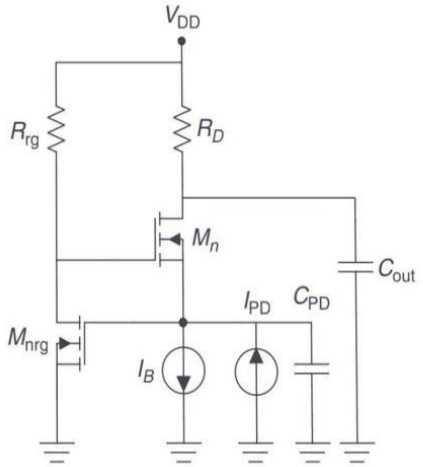

Fig-3: Regulated cascade TIA (RGC-TIA)

D. Inverter TIA (Inv-TIA)

This topology is having a edge in terms of higher gain A_{inv} compared to CS-TIA shown in figure.4 [26] This circuit offers high transconductance gain ($g_{mn}+g_{mp} \approx 2\ g_m$) which gives large Gain-Bandwidth (GBW) product as well as high OL gain (A_{Inv}) with less power consumption. But, compared to CS-TIA this Inv-TIA is better.

OL Gain (A_{inv}) of Inverter Transimpedance amplifier shown as-

$$A_{inv} = -g_m R_O = -(g_{mn} + g_{mp})R_O \quad (9)$$

Here g_{mn} and g_{mp} are transconductances of nmos (M_n) and pmos (M_p) respectively and R_o is the open-loop resistance (R_O).Where R_O is

$$R_o = \frac{R_{DSN}*R_{DSP}}{1+R_{DSN}*R_{DSP}} \quad (10)$$

Here, R_{DSN} and R_{DSP} are the drain to source resistances for the nmos and pmos transistor respectively.

BW of the Inverter trans-impedance amplifier is

$$BW = \frac{A_{inv}+1}{2\,\pi(R_O+R_F)C_{in}} \quad (11)$$

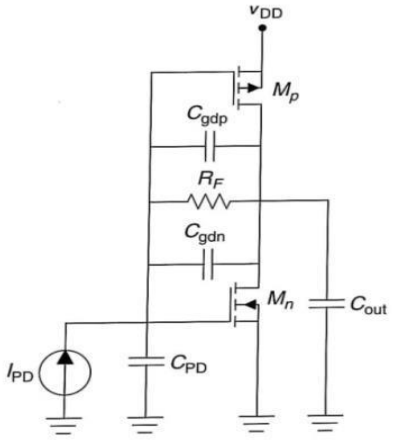

Fig-4: Inverter TIA (Inv-TIA)

E. Current Reuse TIA (CR-TIA)

Topology are configured using CS-TIA(M_{n1}) with shunt feedback resistor (R_F) cascade with CG-TIA(M_{n2}) shown on figure.5 [26].The The amplified output of first stage CS-TIA is applied to CG-TIA to further increase Trans-impedance gain which is taken out from V_{out} . Along with high gain, bandwidth is also increased because of reduced miller capacitance. current reuse provide higher GBW product. Open loop gain (A_1) for CS stage of current reuse TIA is

$$A_1 = -g_{mn1}R_{CS} \quad (12)$$

Here Rcs is the parallel combination of R_{DS1}, R_{DS2} and inverse of g_{mn2}

Open loop gain (A_2) for CG stage (A2) of current reuse TIA is

$$A_2 = g_{mn2}\left(\frac{R_{DSP}R_{DSN2}}{R_{DSP}+R_{DSN2}}\right) \quad (13)$$

Bandwidth of current reuse-TIA is given by

$$\frac{A_1+1}{2\pi f C_{pd}(R_{CS}+R_F)} \quad (14)$$

Where R_{cs} - total drain resistance of M_{n1}, A_1 and A_2.

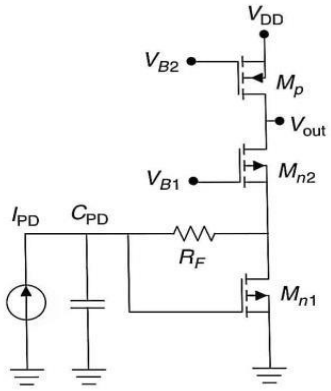

Fig-5: Current Reuse-TIA (CR-TIA)

F. Inverter-Cascode (InvCas-TIA)

Configuration is shown in figure.6 [26]. Here NMOS (M_{n2}) and PMOS (M_{p2}) transistor are connected in series with M_{p1} and M_{n1} inverter transistor. In InvCas-TIA voltage gain is higher than Inv-TIA because of high output resistance of InvCas-TIA, also transimpedance gain is somewhat also higher because of high voltage gain. For two reason the bandwidth of InvCas-TIA is higher, First miller effect and second high voltage gain InvCas Transimpedance amplifier. Gain and Bandwidth can be calculated by:

OL Gain (A_{InvCas}) of Inverter Cascode Transimpedance Amplifier is shown as-

$$A_{InvCas} = -g_m R_o \quad (15)$$

And, Bandwidth of Inverter cascode is

$$BW = \frac{A+1}{2\pi(R_O+R_F)C_{pd}} \quad (16)$$

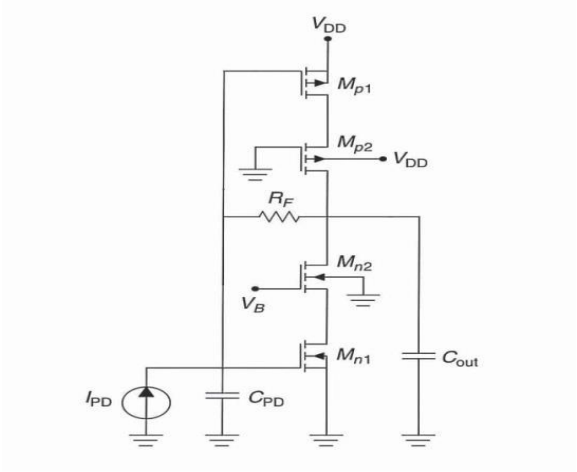

Fig-6: Inverter Cascode-TIA

G. Current-reuse (CR) RGC TIA

CR RGC TIA configuration ,a regulated cascode TIA (RGC-TIA) are widely used reason being it's low input impedance but for further reducing the low input impedance current reuse technique is used in RGC-TIA shown in figure.7.[26] This CR-RGC-TIA increases the trans-conductance by $2g_m = (g_{mp} + g_{mn})$ that is double of RGC TIA [31] Its gain and bandwidth are shown below :

OL Gain of common source (CS) amplifier (A_{CS}) and of RGC (A_{RGC}) amplifier are:

$$A_{CS} = -g_{mn1}R_{CS} \quad (17)$$

Where Rcs is the parallel combination of R_{ON1}, R_{ON2} and inverse of gmn2

$$A_{RGC} = g_{mn2}\frac{(R_{DSP1}R_{DSN2})}{(R_{DSP1}+R_{DSN2})} \quad (18)$$

Bandwidth (BW) of current reuse regulated cascode TIA is as-

$$BW = \frac{A_{CS}+1}{2\pi f C_{pd}(R_{CS}+R_F)} \quad (19)$$

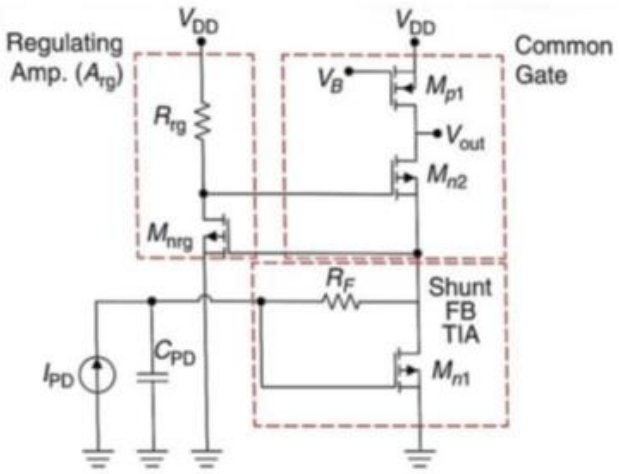

Fig-7: Current Reuse-RGC-TIA

Above shown topologies of trans-impedance amplifier shows the pros and cons on the basis of parameter like gain and bandwidth.

III. RECENT ADVANCEMENTS

In this section we have discussed some of the latest research work has been shown in this area which is based on increasing the bandwidth (BW) and gain. The effect of parasitic of photodiode capacitance make's it arduous to get large bandwidth in TIA. The TIA presented in [37] uses shunt-shunt feedback topology to enhance the Trans-impedance amplifier BW. For enhancing the Bandwidth of TIA, Dynamic threshold MOS transistor (DTMOS) can also be used [9].In [32] using DTMOS method to increase the trans-conductance of the MOS which in turn increases the bandwidth using the composite transistor structure. The gain of TIA can also be increased using floating gate metal oxide semiconductor **(**FGMOS) in [10]. The Bandwidth and phase margin (PM) can be significantly increased in [17] by replacing feedback resistor with Tee network circuit. The TIA presented in [33] uses a floating-active inductor (FAI) which is based on gyrator-C structure with a combination of capacitive degeneration, broadband Matching Network, and Regulated cascode to enhance bandwidth and Gain.

So, There is several ways to attain desired result in terms of it's gain and bandwidth (BW) by analyzing and studying the resent work in this field.

IV. FUTURE SCOPE

Design of TIA need to be optimized carefully for the Trade-offs such as BW, gain, noise, as well as power consumption. For low voltage applications, Low voltage circuit techniques such as Floating gate MOS (FGMOS), Quasi floating gate MOS (QFGMOS), bulk driven technique, Dynamic Threshold MOS etc can be used as well as for minimizing the power consumption these technique can be useful. Various Bandwidth extension techniques such as shunt peaking and Capacitive Degeneration along with many circuit techniques can be applied in a TIA to improve performance. Also for improving the bandwidth demands in TIA cascading can be done of different stages that will enhance the gain and also improves the parasitic capacitance effect.

Table-I. Performance Comparison of Various Topologies of TIA

Ref. No	Year	Technology (CMOS)	TIA Gain (dBΩ)	Bandwidth (GHz)	Power/Supply (Volts)	Topology/Technique
[20]	2004	0.6 µm	54	9.2	2.5 V	Interstage matching network technique
[8]	2006	0.18 µm	52	7.6	2 V	Regulated cascode
[24]	2007	0.18 µm	53	8	1.8 V	Regulated cascode
[30]	2010	0.18 µm	54.6	**7**	1.8 V	Common gate with active feedback
[28]	2011	0.18 µm	40	8.69	1.8 V	RGC- Resistive feedback, source follower and capacitive degeneration.
[19]	2013	0.40 µm	47	8	1.1 V	Inverter, active CD feedback (ICDF-TIA)
[17]	2014	0.65 µm	52	**50**	1.2 V	Differential,peaking technique , RGC input stage with a shunt-feedback.
[34]	2015	0.18µm	50	7	1.5V	Regulated Cascode (RGC)
[5]	2015	0.18µm	61	15	3.3 V	Regulated Cascode
[15]	2015	0.13 µm	61.6	2	1.5 V	Current Reuse, inductor peaking technique
[12]	2016	0.18µm	1.8kΩ	7.2	-	Regulated Cascode, multilevel active feedback (MLAF) structure, inductorless CMOS differential TIA.
[7]	2017	0.18µm	59	7.9	1.8 V	active voltage-current feedback,
[10]	2017	0.18µm	37.7	13.5	1 V	FGMOS, active feedback and shunt peaking network.
[4]	2018	0.90 µm	40.5	7	1 V	active inductive peaking at output load
[2]	2018	0.65 µm	**62**	11	-	regulated cascode (RGC), current reuse strategy
[21]	2018	0.18 µm	56.8	5	1 V	FGMOS,Wilson current mirror
[3]	2019	0.18 µm	49.7	9.2	1.8V	RGC Structure with MOS-based Immittance Converter (MIC)
[13]	2020	0.90 µm	40.6	3.7	1.2V	RGC , level shifter and a common source structure

V. CONCLUSION

Apart from topology device technology, considering the bandwidth and gain, different TIA topologies. has been studied and presented. FGMOS provides best result in terms of High gain, low power supply, Bandwidth and power dissipation. Common Gate TIA and Regulated Cascode TIA provide best results in terms of Higher Bandwidth and minimum power consumption. Likewise in terms of Current Reuse RGC gives high transimpedance across a large bandwidth. Similarly in terms of low power consumption,

Higher gain and High gain-Bandwidth product Inverter Cascode TIA and Regulated cascode TIA seems to be a good choice. To achieve the best characteristics by introducing various bandwidth extension technique, these topologies can be further improved.

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AUTHOR PROFILE

Vineeta Singh, received bachelor’s degree (Hons.) in Electronics from Shaheed Rajguru college of Applied Science For Women (Delhi university), New Delhi, India and M.Sc degree in Electronics from Kurukshetra University, Haryana, India. She is currently pursuing the M.Tech degree in VLSI Design from Indira Gandhi Delhi Technical University For Women (IGDTUW), New Delhi, India. Areas of Interest are Low voltage CMOS Circuits, VLSI Circuits and Analog Circuits.

Sarika Parihar, received bachelor’s degree in Computer science from Jai narain college of technology and science, Bhopal, India. She is currently pursuing the M.Tech degree in VLSI Design from Indira Gandhi Delhi Technical University For Women (IGDTUW), New Delhi, India. Areas of Interest are Low voltage Analog design, CMOS Circuits, VLSI Circuits and Analog Circuits.

Prof. Vandana Niranjan is working as Professor in the Department of Electronics and Communication Engineering at Indira Gandhi Delhi Technical University Delhi, India. She graduated in the year 2000 and received her B.E. degree in Electronics and Communication Engineering from Government Engineering College (now University Institute of Technology of Rajiv Gandhi Proudyogiki Vishwavidyalaya) Bhopal. In the year 2002, she received her M.Tech degree from the Department of Electronics and Communication Engineering at Indian Institute of Technology (IIT) Roorkee with VLSI Design as specialization. In the year 2015, she was awarded her Ph.D degree in the area of Low Voltage VLSI Design from University School of Engineering & Technology, GGSIP University Delhi. She has a teaching and research experience of approximately 20 years at Indira Gandhi Delhi Technical University Delhi. Her areas of interest includes MOSFET body bias techniques and Low-voltage Low-Power Analog CMOS circuit design. She has several publications to her credit in various international journals and conferences and Book chapters.