Design of Carry Select Adder using BEC and Common Boolean Logic

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Abstract: Carry Select Adder (CSLA) is known to be the fastest adder among the conventional adder structure, which uses multiple narrow adders. CSLA has a great scope of reducing area, power consumption, speed and delay. From the structure of regular CSLA using RCA, it consumes large area and power. This proposed work uses a simple and dynamic Gate Level Implementation which reduces the area, delay, power and speed of the regular CSLA. Based on a modified CSLA using BEC the implementation of 8-b, 16-b, 32-b square root CSLA (SQRT CSLA) architecture have been developed. In order to reduce the area and power consumptionin a great way we proposed a design using binary to excess 1 converter (BEC). This paper proposes an dynamic method which replaces a BEC using Common Boolean Logic.

Keywords: SQRT CSLA, BEC, CBL.

I. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speedof addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it usesmultiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III. This brief is structured as follows. Section II deals with the delay and area evaluation methodology of the basic adder blocks. Section III presents the detailed structure and the function of the BEC logic. The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [5], [6]. The delay and area evaluation methodology of the regular and modified SQRT CSLA are presented in Sections IV and V, respectively. The ASIC implementation details and results are analyzed in Section VI. Finally, the work is concluded in Section VII.

II. DELAY AND AREA EVALUATION METHODOLOGY

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1.The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND,OR, and Inverter, each having delay equal to 1 unit and areaequal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.
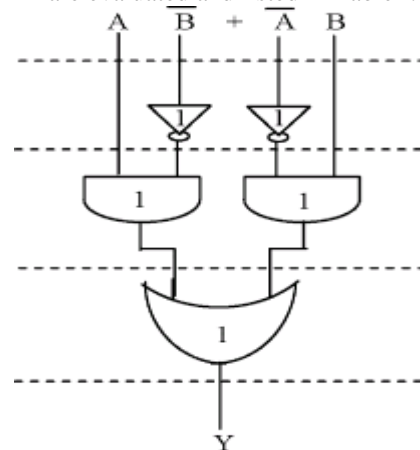

Fig. 1. Delay and Area evaluation of an XOR gate.

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Table I - Delay and Area Count of The Basic Blocks of CSLA

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

III. BEC- BCD TO EXCESS-1 CONVERTER

As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 2 and Table II respectively.
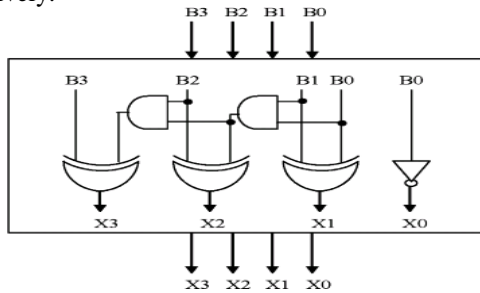

Fig. 2. 4-b BEC.

Fig. 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output.

Table II - Function Table of the 4-B Bec

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~NOT, & AND, ^XOR)

$X0=\sim B0$
$X1=B0 \wedge B1$
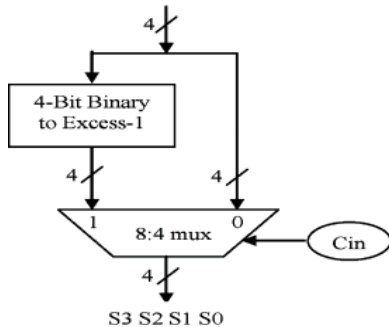$X2=B2 \wedge (B0\&B1)$ $X3=B3 \wedge (B0\&B1\&B2)$

Fig. 3. 4-b BEC with 8:4 mux.

IV. DELAY AND AREA EVALUATION METHODOLOGY OF 16-B SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Fig. 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 5, in which the numerals within [] specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows,
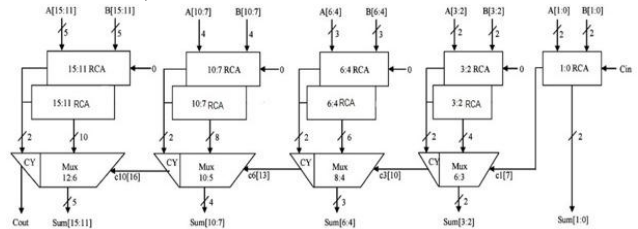

Fig. 4. Regular 16-b SQRT CSLA.

The group2 [see Fig. 5(a)] has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection c1[time(t)=7] of 6:3 mux is earlier than s3[t=8] and later than s2[t=6]. Thus sum 3[t=11] is summation of s3 and mux[t=3] and sum2[t=10] is the summation of c1 and mux.

Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows:

$\{c6,sum[6:4]\}=c3[t=10]+$
mux
$\{c10,sum[10:7]\}=c6[t=13]+mux$
$\{cout,$
$sum[15:11]\}=c10[t=16]+mux.$
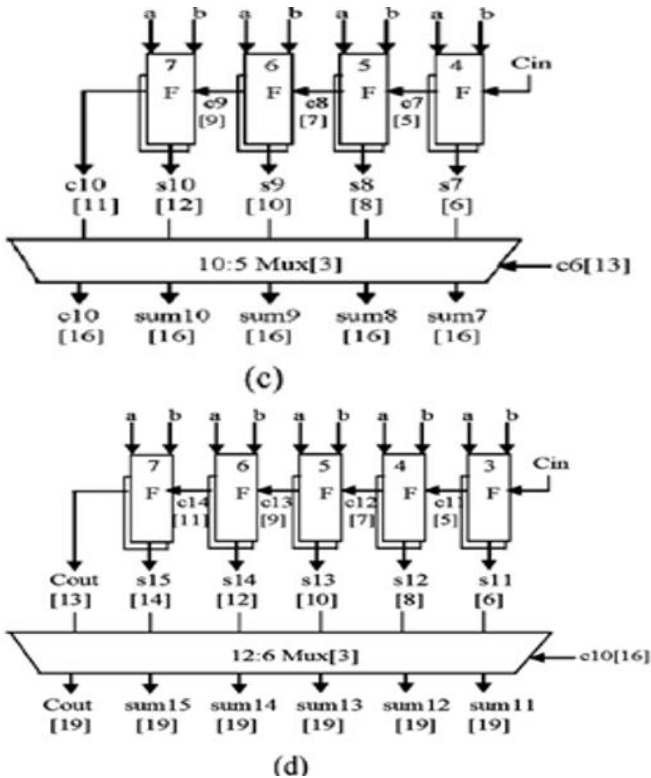Mux=12(3*4).

(a)   (b)

(c)

(d)
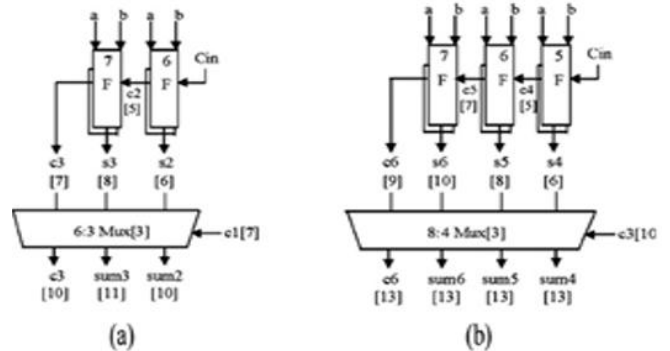
Fig. 5. Delay and area evaluation of regular SQRT CSLA: (a)group2, (b) group3, (c) group4 and (d) group5. F is a Full Adder.

Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed

Table III- Delay and Area Count of RegularSqrt CSLA Groups

DELAY AND AREA COUNT OF REGULAR SQRT CSLA GROUPS

Group	Delay	Area
Group2	11	57
Group3	13	87
Group4	16	117
Group5	19	147

V. DELAY AND AREA EVALUATION METHODOLOGY OF MODIFIED 16-B SQRT CSLA

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Fig. 6. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 7. The steps leading to the evaluation are given here.
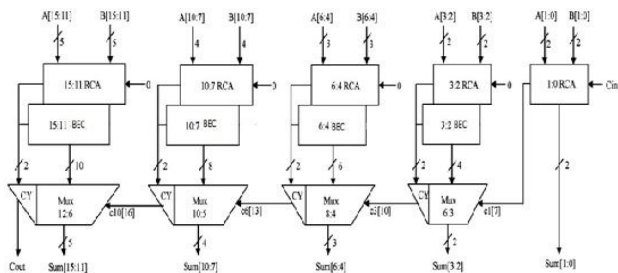

Fig. 6. Modified 16-b SQRT CSLA. The parallel RCA withCin=1 is replaced with BEC

The one set of 2-b RCA in group2 has 2 FA for Cin=1 and the other set has 1 FA and 1 HA for Cin=0. Based on the area count of Table I, the total number of gate counts in group2 is determined

Gate Count=57(FA + HA + Mux).
FA=39(3*13).
HA=6(1*6).

The group2 [see Fig. 7(a)] has one 2-b RCA which has 1 FA and 1 HA for Cin=0. Instead of another 2-b RCA with Cin=1 a 3-b BEC is used which adds one to the output from 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c_1[time(t)=7] of 6:3 mux is earlier than the s_3[t=9]and c_3[t=10] and later than the s_2[t=4]. Thus, the sum3 and final (output from mux) are depending on s_3 and mux and partial c_3(input to mux) and mux, respectively. The sum2 depends on c_1 and mux.

(a)   (b)
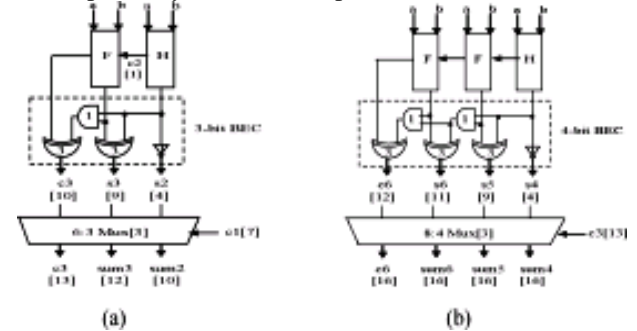
1) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and mux delay.
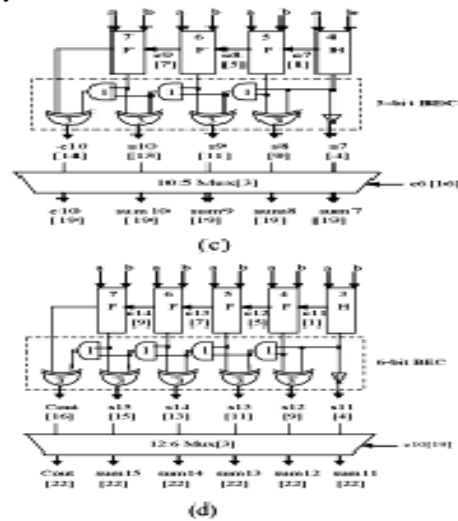

(c)

(d)

Fig. 7. Delay and area evaluation of modified SQRT CSLA: (a) group2, (b) group3, (c) group4, and (d) group5.

H is a Half Adder 3) The area count of group2 is determined as follows in Table IV.

Table IV - Delay and Area Count of ModifiedSqrt CSLA

Gate count = 43 (EA + HA + Mux + BEC)

EA = 13 (1 * 13)

HA = 6 (1 * 6)

AND = 1

NOT = 1

XOR = 10 (2 * 5)

Mux = 12 (3 * 4).

DELAY AND AREA COUNT OF MODIFIED SQRT CSLA

Group	Delay	Area
Group2	13	43
Group3	16	61
Group4	19	84
Group5	22	107

Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table IV.

Comparing Tables III and IV, it is clear that the proposed modified SQRT CSLA saves 113 gate areas than the regular SQRT CSLA, with only 11 increases in gate delays. To further evaluate the performance, we have resorted to ASIC implementation and simulation.

VI. ASIC IMPLEMENTATION RESULTS

The design proposed in this paper has been developed using Verilog-HDL and synthesized in Cadence RTL compiler using typical libraries of TSMC 0.18 um technology. The synthesized Verilog netlist and their respective design constraints file (SDC) are imported to Cadence SoC Encounter and are used to generate automated layout from standard cells and placement and routing [7]. Parasitic extraction is performed using Encounter's Native RC extraction tool and the extracted parasitic RC (SPEF format) is back annotated to Common Timing Engine in Encounter platform for static timing analysis. For each word size of the adder, the same value changed dump (VCD) file is generated for all possible input conditions and imported the same to Cadence Encounter Power Analysis to perform the power simulations. The similar design flow is followed for both the regular and modified SQRT CSLA.

Table V exhibits the simulation results of both the CSLA structures in terms of delay, area and power. The area indicates the total cell area of the design and the total power is sum of the leakage power, internal power and switching power.

Table V - Comparison of The Regular andModified Sqrt CSLA

Word Size	Adder	Delay (ns)	Area (um²)	Leakage Power	Switching power	Total power*	Power-Delay Product(10⁻¹⁵)	Area-Delay Product(10⁻¹⁵)
					Power (uW)			
8-bit	Regular CSLA	1.719	991	0.007	101.9	203.9	350.5	1703.5
	Modified CSLA	1.958	895	0.006	94.2	188.4	368.8	1752.4
16-bit	Regular CSLA	2.775	2272	0.017	263.7	527.5	1463.8	6304.8
	Modified CSLA	3.048	1929	0.013	235.9	471.8	1438.0	5879.6
32-bit	Regular CSLA	5.137	4783	0.036	563.6	1127.3	5790.9	24570.2
	Modified CSLA	5.482	3985	0.027	484.9	969.9	5316.9	21845.7
64-bit	Regular CSLA	9.174	9916	0.075	1212.4	2425.0	22246.9	90969.3
	Modified CSLA	9.519	8183	0.057	1025.0	2050.1	19514.9	77893.9

*Total power = leakage power + Internal power + Switching power

The percentage reduction in the cell area, total power, power-delay product and the area–delay product as function of the bit size are shown in Fig. 8(a). Also plotted is the percentage delay overhead in Fig. 8(b). It is clear that the area of the 8-, 16-, 32-, and 64-b proposed SQRT CSLA is

reduced by 9.7%, 15%, 16.7%, and 17.4%, respectively. The total power consumed shows a similar trend of increasing reduction in power consumption 7.6%, 10.56%, 13.63%, and 15.46 % with the bit size.
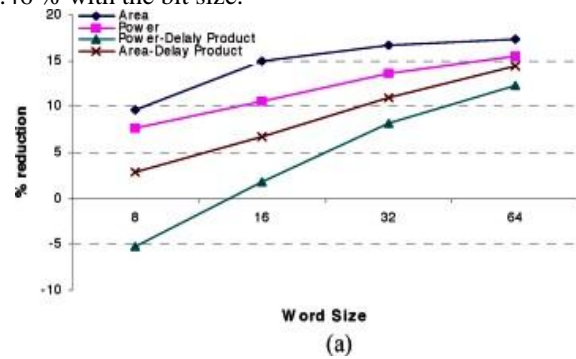

Fig. 8. (a) Percentage reduction in the cell area, total power,power–delay product, and area–delay product.

Interestingly, exhibits a similarly decreasing trend with bit size. The delay overhead for the 8, 16, and 32-b is 14%, 9.8%, and 6.7% respectively, whereas for the 64-b it reduces to only 3.76%. The power–delay product of the proposed 8-b is higher than that of the regular SQRT CSLA by5.2% and the area-delay product is lower by 2.9%. However, the power-delay product of the proposed 16-b SQRT CSLA reduces by 1.76% and for the 32-b and 64-b by as much as 8.18%, and 12.28% respectively. Similarly the area-delay product of the proposed design for 16-, 32-, and 64-b is also reduced by 6.7%, 11%, and 14.4% respectively.
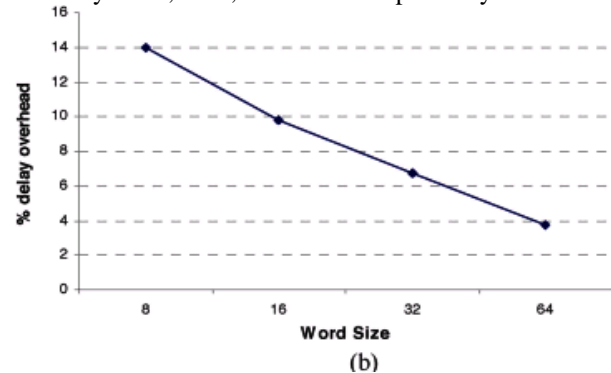

Fig. 8. (b) Percentage of delay overhead.

VII. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere trade off of delay for power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation.

It would be interesting to test the design of the modified 128-b SQRT CSLA.

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